CV SUMMARY - CRISTINA SILVANO

EDUCATION

1999 **PhD Degree** in Information Engineering, Università degli Studi di Brescia, Italy.
1987 **Master of Science Degree** in Electrical Engineering, Politecnico di Milano, Italy (Final Grade 100/100).

CAREER

2018 – present **Full Professor** in Computer Engineering, Dept. of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano, Italy
2002 – 2018 **Associate Professor** in Computer Engineering, DEIB, Politecnico di Milano, Italy
2000 – 2002 **Assistant Professor** in Computer Science, Dept. of Computer Science, Univ. degli Studi di Milano, Italy
1999 – 2000 **Post-Doc Researcher** (Assegnista di Ricerca), DEIB, Politecnico di Milano, Italy
1999 **Post-Doc Researcher** at CEFRIEL, Milano, Italy
1996 – 1998 **Ph.D. Student,** Università degli Studi di Brescia, Italy
1987 – 1996 **Design Engineer** (**Senior Design Engineer** since 1993), R&D Labs of Group Bull, Pregnana M., Italy

RESEARCH INTERESTS

Principal Investigator of the ANTAREX EU research project group focused on application autotuning and adaptivity for energy-efficient High Performance Computing systems. My research interests are focused on:

- **Computer Architectures:** energy-efficient computer architectures, embedded architectures, manycore architectures, Networks-on-Chip, technology-aware architecture design, VLIW (Very Long Instruction Word) processor architectures.
- **Electronic Design Automation:** low-power design for embedded architectures, design space exploration of energy-efficient computer architectures, application autotuning and runtime management for manycore systems and High-Performance Computing, compiler autotuning based on machine learning.

LEADERSHIP IN RESEARCH PROJECTS

2015 – 2018 **Project Coordinator** (Principal Investigator), EU Project **ANTAREX** (3 M€), Call H2020-FET-HPC-1-2014 Partners: POLIMI, ETH Zurich, Univ. of Porto, INRIA; CINECA, IT4Innovations, Dompé, Sygic.
2010 – 2013 **Project Coordinator** (Principal Investigator), EU Project **2PARMA** (2.7 M€), Call FP7-ICT-4-2009 Partners: POLIMI, STMicro, HHI-Fraunhofer Inst., IMEC, Univ. of Athens, RWTH Aachen Univ., Synopsys
2008 – 2010 **Project Coordinator** (Principal Investigator), EU Project **MULTICUBE** (2.1 M€), Call FP7-ICT-1-2007 Partners: POLIMI, DS2, STMicro, IMEC, ESTECO, USI, Univ. Cantabria, Chinese Academy of Sciences.
2006 – 2008 **Principal Investigator,** Research Grant funded by STMicroelectronics (60 K€)
2003 – 2005 **Principal Investigator,** Research Grant funded by STMicroelectronics (60 K€)

SCIENTIFIC PRODUCTION AND METRICS

- **Scientific Productivity:** More than **160** publications (**157** entries on Scopus):
  - Co-author of **31** top-ranked journal papers including **19 IEEE/ACM Transactions** and **1 ACM Computing Survey;**
  - Co-author of more than **90** scientific publications on peer-reviewed conferences including top-level conferences (such as DAC, ICCAD, ASP-DAC, DATE, CODES-ISSS, CASES);
  - Co-editor of **3** scientific books: "Near Threshold Computing", Springer (2015), "Low-Power Networks-on-Chip", Springer (2010), "Multi-objective design space exploration of multiprocessor SoC architectures", Springer (2011);
  - Co-author of **2** scientific books: "Automatic Tuning of Compilers using Machine Learning" Springer (2018), "Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems", Kluwer (2003);
  - Inventor/Co-inventor of **11** patent applications with Group Bull and STMicro (**7** out of **11** already granted).
- **Publication Impact:** Based on Google Scholar: h-index **31** citations **3568**
  Based on Scopus: h-index **23** citations **1707**

AWARDS AND RECOGNITIONS (SELECTION)

2017 **IEEE Fellow** "for contributions to energy-efficient computer architectures"
2013 2PARMA Project recognized as **Success Story** of the Directorate General DG-CONNECT of the European Commission.
2010 **HiPEAC 2010 Paper Award** as co-author of a paper published at DAC 2010.
2008 **Recipient** co-author of one of "The Most Influential Papers of 10 Years DATE".
2008 **ACM Recognition of Service Award** for contributions as General Co-chair MICRO-41
2008 **ACM Best Paper Award** at ACM Symposium on Applied Computing 2008.
1991 **Bull Technical Award** "for contributions to an integrated CAD framework for complex ASIC design"

INVITED TALKS AND SEMINARS (SELECTION)

Over **25** invited talks/seminars at international venues. Among them:

2017 Keynote Speaker at HeteroPar2017 Workshop, co-located to EuroPar Conference, Santiago, Spain
2016 Seminar at Brain Inspired Computing Group, IBM Research, Austin
2016 Seminar at the University of Texas at Austin, ECE, Computer Architecture Seminar Series
2015 Keynote Speaker at the 13th IEEE Int. Conf. EUC 2015 / 18th IEEE Int. Conf.CSE 2015
2012 Seminar at Intel Labs, Santa Clara, CA, USA

2010 Seminar at University of California Riverside, Dept. of Computer Science & Engineering
2010 Seminar at University of California Irvine, Dept. of Computer Science & Engineering
2010 Seminar at Delft Technical University, Computer Engineering Colloquium Series
2009 Seminar at Princeton University, Dept. of EE, Computer Engineering Seminar
2009 Seminar at HP Labs, Palo Alto, CA, USA

TEACHING EXPERIENCE (SELECTION FROM 2008)

Balanced effort in teaching at **B.Sc.** and **M.Sc. levels**. Current courses held as Associate Professor at Politecnico di Milano:

- Advanced Computer Architectures (5 credits), M. Sc. in Computer Engineering, Politecnico di Milano (Course offered in English), Leonardo Campus, **180+** students
- Advanced Computer Architectures (5 credits), M. Sc. in Computer Engineering, Politecnico di Milano (Course offered in English), Como Campus, **60+** students.
- Operating Systems (5 credits), B.Sc. in Computer Engineering, Politecnico di Milano, Como Campus, **70+** students

INSTITUTIONAL RESPONSIBILITIES (SELECTION)

2015 – present **Project Manager** of the IBM/POLIMI Collaborative Innovation Center on Big Data Analytics
2003 – present **Member** of the Committee on Graduate Admissions in Computer Engineering, Politecnico di Milano, Como Campus (since 2003), Leonardo Campus (since 2015).
2002 – present **Member** of the Committee on Undergraduate Study Plans and Transfers in Computer Engineering, Politecnico di Milano, Como Campus.
2002 – present **Advisor/Co-advisor** of **60+** Master Students in Computer Engineering, School of Industrial and Information Engineering, Politecnico di Milano

SUPERVISION OF DOCTORAL AND POSTDOCTORAL STUDENTS

2002 – present **Advisor/Co-advisor** of **10** Doctoral Students at Politecnico di Milano, **2** Doctoral Students at Università della Svizzera Italiana (USI) and **2** Postdoctoral Students at Politecnico di Milano.
2009 – present **Opponent Member** of **9** Doctoral Examination Committees at TU Athens, Univ. of Verona, Norwegian Univ. of Science & Tech., RWTH Aachen Univ., TU Eindhoven, TU Delft, Univ. Politecnica de Catalunia.

ORGANIZATION OF SCIENTIFIC MEETINGS (SELECTION)

Active contributor to the scientific community serving regularly in the Technical Program Committee of several top-level conferences such as DAC, ICCAD, DATE, NOCS, PACT, MICRO, ASAP and FPL. Among them:

2015 – 2017 **Track Chair/Track Co-chair,** IEEE/ACM Design and Test in Europe Conference (DATE)
2015 – 2016 **Track Chair,** IEEE/ACM Int. Conference on Computer-Aided Design (ICCAD)
2012, 2015 **Sub-committee Chair,** IEEE/ACM Design Automation Conference (DAC)
2015 **Program Chair,** 25th Int. Conf. on Field Programmable Logic and Applications, London, UK
2012 **Program Co-Chair,** 23rd IEEE Int. Conf. on Application-specific Systems, Arch. and Processors (ASAP), Delft, NL
2010 **Program Co-Chair,** IEEE Symposium on Application Specific Processors, co-located with DAC, Anaheim, CA
2009 **General Co-Chair,** IEEE Symposium on Application Specific Processors, co-located with DAC, San Francisco, CA
2008 **General Co-Chair,** 41st IEEE/ACM Int. Symposium on Micro-architecture, Como, IT

COMMISSIONS OF TRUST (SELECTION)

2017 – present **Steering Group Member,** UK Engineering and Physical Sciences Research Council, UK
2017 – present **Expert Reviewer,** FWO (Research Foudation Flanders), BE
2016 – present **Expert Reviewer,** Swiss National Science Foundation, CH
2015 – present **Associate Editor,** ACM Transactions on Architecture and Code optimization (TACO)
2013 – 2015 **Associate Editor,** MICPRO Journal, Embedded HW Design (Microprocessor and Microsystems), Elsevier
2013 – 2015 **Independent Expert Reviewer,** European Commission, ARTEMIS JU Project
2010 **Expert Reviewer,** Programme Blanc Int., Agence Nationale de la Recherche, FR
2009 – 2013 **Independent Expert Reviewer,** European Commission, FET-Open Programme
2008 – 2009 **Member/Chair** of the Review Panel for Computer Science, Academy of Finland, FL
2007 **Primary Evaluator,** INRIA (French National Institute for Computer Science), FR
2005 – 2014 **Independent Expert Reviewer,** EU Commission, FP6 and FP7 Projects and Network of Excellence HiPEAC

INDUSTRIAL EXPERIENCE

1993 – 1994 **Visiting Engineer** at IBM Somerset Design Center, Austin (TX - USA).
1992 – 1996 **Member of Bull-IBM Design Team** of the first worldwide multiprocessor system based on IBM PowerPC, commercialized as Bull Escala UNIX Servers and as IBM RS/6000 Multiprocessor Servers.
1990 **Visiting Engineer** at VLSI Technology, in Munich (D) and in S. Jose (CA-USA)
1988 – 1989 **Visiting Engineer** at Honeywell-Bull R&D Labs, Billerica (MA - USA)
1987 – 1996 **Design Engineer** (since 1993 **Senior Design Engineer**) at R&D Labs of Group Bull in Italy.

CURRICULUM VITAE - CRISTINA SILVANO

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1. PERSONAL DATA AND CAREER

Cristina Silvano, Ph.D.
Full Professor
Politecnico di Milano
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Tel.: +39-02-2399-3692
Email: cristina.silvano@polimi.it
Home page: http://home.deib.polimi.it/silvano/
Born in Milan (Italy), December 25th, 1961.
Nationality: **Italian.** Resident in Milan (Italy).
Languages: **Italian** (mother tongue); **English** (fluent); **French** (good).

My career is twofold. In 1987, after graduation at Politecnico di Milano, I have started my ***industrial career*** as Design Engineer (then upgraded as Senior Design Engineer) at the R&D Labs of Group Bull (Italy) spending several periods abroad as Visiting Engineer. Almost a decade later, to follow my interests in the scientific research and my attitude towards teaching, I have started my ***academic career*** as Ph.D. student at Università degli Studi di Brescia (Italy). After my Ph. D., attained in 1999, I continued as Post-Doc Researcher at CEFRIEL and at Politecnico di Milano, Assistant Professor at Università degli Studi di Milano (2000-2002) and Associate Professor at Politecnico di Milano (2002-present). In 2017, I was elevated to the grade of **IEEE Fellow** by the IEEE Boards of Directors ***"for contributions to energy-efficient computer architectures".***

1.1. EDUCATION

- **Dottorato di Ricerca in Ingegneria dell'Informazione (Ph.D. in Computer Engineering), Università degli Studi di Brescia (Italy), 1999.** Ph.D. Thesis on: "Power Estimation and Optimization Methodologies for Digital Circuits and Systems", Advisor: Prof. Paolo Gubian, Università degli Studi di Brescia, Co-Advisor: Prof. Donatella Sciuto, Politecnico di Milano.
- **Laurea in Ingegneria Elettronica (Master of Science in Electrical Engineering), Politecnico di Milano, 1987 (Final grade 100/100).** Ms. Thesis on: "Theoretical and numerical study of shallow waters fluid dynamic models", Advisor: Prof. Giovanni Prouse, Politecnico di Milano, Co-Advisor: Prof. Laura Gotusso, Politecnico di Milano.

1.2. ACADEMIC CAREER

- **Full Professor** (from 03/12/2018) in Computer Engineering at Politecnico di Milano, Department of Electronics, Computer Engineering and Bioengineering (DEIB). I annually teach basic and advanced courses on Computer Architectures and Operating Systems. My primary research interests are in the areas of Computer Architecture and Electronic Design Automation, with particular emphasis on power-aware design, design space exploration for embedded architectures, adaptive design and monitoring of applications for manycore architectures, manycore architectures based on Networks-on-Chip, technology-aware manycore architectures and fault tolerant coding techniques.
- **Associate Professor** (01/09/2002 - 02/12/2018) in Computer Engineering at Politecnico di Milano, Department of Electronics, Computer Engineering and Bioengineering (DEIB). I was annually teaching basic and advanced courses on Computer Architectures and Operating Systems. My primary research interests are in the areas of Computer Architecture and Electronic Design Automation.
- **Assistant Professor** (01/10/2000 - 31/08/2002) in Computer Science at Università degli Studi di Milano, Department of Computer Science. I was annually teaching basic and advanced courses on Computer Architectures and Operating Systems. My research activity was mainly focused on power-aware computing for embedder processor architectures.
- **Post-Doc Researcher** (Assegnista di Ricerca) (01/9/1999 - 30/09/2000) at Politecnico di Milano, Dipartimento di Elettronica e Informazione. Main research topic: "Computing Architectures: testing and simulation systems" (Supervisor Prof. D. Sciuto, Politecnico di Milano). My research activities were also related to the research project on *"Power estimation methodologies for VLIW architectures",* in collaboration with STMicroelectronics.

- **Post-Doc Researcher** (01/01/1999 - 31/08/1999) at CEFRIEL (Center for the Research and the Education in Information Engineering, Milan), Electronic Design Automation Area. My research activity was mainly part of the research project TOSCA (Tools for System Co-design Automation) and the European Project No. 26796 PEOPLE (Power Estimation for fast exPLoration of Embedded systems) under the supervision of Prof. D. Sciuto.

- **Ph.D. Student** (01/03/1996 – 31/12/1998) at Università degli Studi di Brescia (Italy), Dipartimento di Elettronica per l'Automazione. My research activity was mainly focused on power estimation and optimization methodologies for embedded architectures. Ph.D. defense held in 1999.

1.3. INDUSTRIAL CAREER

From May 1987 to February 1996, I was employee at the **R&D Laboratories of Groupe Bull** (also known as Bull HN Information Systems), Pregnana Milanese (Italy) where I held the position of **Design Engineer** up to March 1993 and **Senior Design Engineer** up to February 1996. During my experience at Groupe Bull, I have been involved in the following research and development activities:

- From September 1988 to October 1990, I was part of the design team of a full-custom 32-bit Central Processing Unit including a virtual memory management unit. The CPU was designed for a system based on the GCOS6 Bull proprietary OS.
  - **Visiting Engineer** at the **Honeywell Bull R&D Labs, Billerica (MA - USA)** in Fall 1988 and in Spring 1989.
  - **Visiting Engineer** at the VLSI design center of **VLSI Technology Inc., Munich (Germany)** in February-March 1990
  - **Visiting Engineer** at the VLSI design center of **VLSI Technology Inc. in S. Jose (CA-USA)** in April 1990.
  - For my contribution to the microprocessor design and verification, I received the **"1991 Bull Technical Award"**.
- In 1990, I designed a Dual Port SRAM module generator based on a process-independent design methodology. The generator has been used to synthesize two embedded memories integrated in a VLSI circuit designed for the European project ESPRIT2 -IDPS (Integrated Design and Production System) No. 5075 (1990-1992). In 1992, I have applied as co-inventor of a hierarchical and modular memory architecture in one **European patent** [P1-EU] granted in 1997.
- From 1991 to July 1992, I was with the Bull Advanced Technology Group, responsible for the introduction of new technologies and methodologies in the design of integrated circuits for Bull computer systems.
- Since August 1992, I was member of the **Bull-IBM Research (Austin-US)** design team of the chip set for the Bull Escala multiprocessors, which are symmetric and scalable systems based on shared memory architecture and composed of two to eight processors. The Escala systems have been **the first worldwide multiprocessors based on the PowerPC architecture** (introduced in 1992 by the Apple-IBM-Motorola alliance, then generating the PowerPC 601, 604e e 620 processors). The first implementation of the architecture was the PowerPC 601 released by IBM in 1992. The Escala systems have been fully developed by a Bull-IBM joint team at the R&D Bull Labs and then commercialized as **Bull Escala UNIX Servers** and **IBM RS/6000** Symmetric Multiprocessor Servers (named also as **RS/6000 POWERservers, RS/6000 POWERstation** and then renamed as **eServer pSeries** in October 2000). During the Bull-IBM joint project, I also was **Visiting Engineer** at **IBM Somerset Design Center, Austin (TX - USA)** in Fall 1993 and in Spring 1994. For the research and development of the Escala/RS6000 multiprocessor systems, my main contributions were:
  - From August 1992 to May 1993**,** I was in the design team of the chip-set implementing the 64-bit data cross bar architecture, named **Power Scale,** connecting four processor nodes (including two processors each), the I/O node (including two I/O channels), and the shared memory. The Power Scale architecture has been adopted by many commercial series of the Bull Escala servers. The chip-set includes a new error detection and correction code to improve system reliability and data integrity. From this code, I developed the construction techniques for a new class of codes for computer memory sub-systems. For the new class of codes, I applied as Inventor in one **European Patent (granted in 1998)** [P2-EU] and in one **US Patent (granted in 1996)** [P2-US].
  - From June 1993 to July 1994, I was in the design team of a 120K gates VLSI circuit with the functionality

of Secondary Cache Controller for both PowerPC 601 and 604 processors. The circuit implements the cache coherency mechanism both vertically (between the different cache levels of each processor) and horizontally (among different processors). The cache coherency is based on the MESI protocol.

- From September 1994 to December 1995, I was in the team for the design and simulation of a 230K gates VLSI circuit with the functionality of Memory Controller**,** based on a shared and interleaved memory sub-system. The circuit manages also the data-cross bar architecture, Power Scale, for the new series of multiprocessor systems: Escala-E and Escala-T. More in detail, The Escala-E servers support up to two processors (PowerPC 604e or 620), the shared memory configurable from 16MB to 2 GB, and a single 64-bit PCI bus. The Escala-T servers support up to four processors (PowerPC 604e or 620), the shared memory configurable from 32 MB to 3 GB, and two 64-bit PCI buses.

- During the Academic Years 1993/94 and 1994/95, I also held the position of **Bull Senior Researcher,** supervisor of some Master students in Information Technology at **CEFRIEL** – Research and Training Center in Milano in the Electronic Design Automation area. The activities were partially funded by the European Project EUREKA/JESSI (Joint European Submicron Initiative) – Subprogram Application AC-5.

2. RESEARCH ACTIVITIES

2.1. RESEARCH TOPICS AND MAIN ACHIEVEMENTS

My research is primarily focused on the areas of **Computer Architectures** and **Electronic Design Automation,** with emphasis on the following research topics *(listed hereafter in chronological order).* For each research topic, the most significant achievements are reported with references to my **Publication List.**

2.1.1. Fault Detection and Fault Tolerant Coding Techniques

The research investigates Error Control Coding techniques to improve the fault detection and fault tolerance in computing systems. Main goals of the research are, from one side, the design of a new class of error detection and correction codes and, from the other side, the definition of detection codes for unidirectional errors. Starting from the proposed coding schemes, a set of automatic tools to support the design of the proposed coding techniques has been defined.

Main achievements: My contribution to the field was the introduction of a new class of systematic SEC-DED (Single Error Correction – Double Error Detection) codes with single byte error detection capability published in **IEEE Trans. on Information Theory 1995** [J31][1]. An automatic code generation framework was developed and published in **IEEE Trans. on VLSI 1998** [J28]. For the new class of codes, I have been designated as **inventor** in both the **European Patents** [P2-EU] granted in 1998 and in the **US Patent** [P2-US] granted in 1996. An implementation of the new class of error detection and correction codes has been part of the PowerScale architecture commercially adopted by the **Bull Escala** and **IBM RS6000** multiprocessor servers.

2.1.2. Power-Aware Design for Embedded Architectures

Power dissipation has been identified as the main performance limiter for high-performance processors, while power dissipation limits the capabilities of battery-powered embedded mobile devices and wireless sensor nodes. In 1996, at the beginning of my Ph.D. program (under the supervision of my co-advisors, prof. Paolo Gubian and prof. Donatella Sciuto), I started to investigate on power optimisation and estimation techniques for embedded processor architectures. The main goal of my Ph. D. research was to develop design techniques for the estimation and optimization of the power dissipation of digital circuits and systems. My Ph.D. thesis research represents one of the first efforts to face the problem of power-aware bus encoding for processor-to-memory communication by exploiting spatial-temporal locality.

Main achievements of my Ph.D. thesis related to low-power bus encoding techniques have been published in **IEEE-GLS-VLSI-1997** [C88] and **IEEE/ACM-DATE-1998** [C85]. These two pioneering papers on low-power bus enconding have had a high research impact: so far, they have had **544** citations, still representing *my top ranked papers* based on Google Scholar. Ten years after, the paper presented at **IEEE/ACM-DATE-1998** [C85] has been selected as a chapter of the volume: *"The Most Influential Papers of 10 Years DATE"* [CH12]. For the design of a low-power encoder/decoder architecture (developed in collaboration with STMicroelectronics), I have been designated as co-inventor in the **European Patent Application** [P3-EU] published in 2001 and in the **US Patent Application** [P3-US] published in 2002. The most significant achievements of my Ph.D. thesis on high-level power estimation have been published in **IEEE Trans. on VLSI-1998** [J29] and **JSA-1997** [J30].

Then I started my **post-doc** at Politecnico di Milano (under the supervision of my mentors, prof. Donatella Sciuto and prof. Mariagiovanna Sami) and my research moved towards the investigation of power-aware techniques for embedded architectures based on VLIW (Very Long Instruction Word) pipelined processors. My post-doc research on low-power VLIW architectures has been carried out in collaboration with Vittorio Zaccaria (at that time Ph.D. student at Politecnico di Milano). At that time, research on instruction-level power analysis has just started. Our work was one of the first attempt to define an instruction-level energy model for Very Long Instruction Word (VLIW) pipelined processors. To address the limitations of existing approaches, the main contribution of this pioneering work were: 1) to provide an accurate energy model of the VLIW processor during an instruction-level simulation and 2) to provide power-oriented instruction scheduling at compile time. The most significant results of this work was to develop the first and most comprehensive power estimation framework at the instruction-level validated on an industrial VLIW architecture: the **Lx/ST200** family of VLIW embedded processor cores (developed as a partnership between HP Labs and STMicroelectronics). The **ST200** family (including the ST210, ST220, ST231 processor cores) was widely used for embedded media processing in

[1] Please refer to my Publication List.

a variety of audio, video and imaging consumer products. Another significant result of my Post-Doc research was the definition of an innovative low-power VLIW processor architecture to exploit the pipeline forwarding paths to save power when accessing short-lived variables, avoiding the write-back to the register file. Experimental evidence of the benefits of the proposed architecture has been done on the Lx/ST200 VLIW family. For the low-power forwarding architecture, I have been designed as co-inventor in the **US Patent** [P4-US] **granted in 2005.**

Main achievements: The main achievements of my post-doc research have been published in top-ranked conferences and journals. More in detail, the instruction-level energy model for VLIW pipelined processors has been published in **CODES-2000** [C76], **ICCAD-2000** [C74], **PATMOS-2001** [C70] and then extended to the **IEEE Trans. on CAD-2002** [J26]. Results on the reduction of the complexity of the energy model by introducing the concept of instruction clustering have been presented in **DAC-2002** [C68] then extended in **DAES-2005** [J22]. Results on power optimization of the pipeline forwarding paths and power-aware branch prediction techniques for VLIW have been published in **DATE-2001** [C73], **GLS-VLSI-2003** [C64], **GLS-VLSI-2004** [C61] then extended to **IEEE Trans. on VLSI-2002** [J24] and **Integration-2005** [J23]. Finally, most significant contributions on power-aware VLIW design techniques have been collected in the **scientific book**: *"Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems"* [B5] published in 2003 by Kluwer Academic Publishers.

The research experience on power-aware computing lead me towards one of my primary research paths: design space exploration techniques for energy-efficient computer architectures.

2.1.3. Design Space Exploration of Energy-efficient Computer Architectures

Given the complexity of multi/manycore architectures, system optimization and exploration definitely represent challenging research tasks. A wide range of design parameters must be tuned from a multi-objective perspective, mainly in terms of performance and energy consumption to find the most suitable system configuration for the target application. Multi-objective exploration of the huge design space of multi/manycore architectures needs for automatic Design Space Exploration (DSE) techniques to systematically explore the design choices and to compare them in terms of multiple competing objectives (trade-offs analysis). The aim of my research (carried out mainly in collaboration with Vittorio Zaccaria and Gianluca Palermo at Politecnico di Milano) was to investigate on power/performance trade-offs in application-specific embedded architectures. The exploration techniques are based on multi-objective optimization algorithms and energy/delay estimation metrics. The main goal is to provide an automatic DSE methodology and tool for the analysis of system characteristics and the selection of the most appropriate architectural solution to satisfy power/performance system requirements. A set of heuristic optimization algorithms have been defined to prune the design space to be explored, while a set of response surface modeling techniques have been defined to further speed up the exploration time. The basic idea was defining an analytical response model of the system behavior based on a subset of system simulations to predict the unknown system response. The primary contribution was to define an automatic multi-objective DSE methodology and related framework (**MULTICUBE Explorer**) to tune embedded on-chip platforms finding the best power/performance trade-offs, while meeting system-level constraints and speeding up the exploration process. The **MULTICUBE Explorer** framework leverages a set of open-source tools for the exploration, modeling and simulation to guarantee a wide exploitation of the project results in the embedded system design community. The impact of this research has been demonstrated by the success of the FP7 **MULTICUBE** European projects (2008-2010) carried out under my scientific coordination. In this context, the benefits of the MULTICUBE design methodology and tools have been assessed on industrial use cases provided by **STMicroelectronics** and on **IMEC** virtual platforms.

Main achievements: I am currently ranked among the top research contributors in the area of the design space exploration techniques for multi/many core computing architectures. The most significant results of my research on DSE have been published in top-ranked journals like **DAES-2002** [J27], **DAES-2007** [J18], **IEEE Trans. on CAD 2009** [J14] and **IEEE Trans. on CAD 2012** [J12]. Several papers have also been published in several conferences: **CODES-2001** [C72], **DATE-2003** [C67], **SAC-2003** [C66], **GLS-VLSI-2003** [C65], **PATMOS-2003** [C63], **SAC-2004** [C62], **SASP-2008** [C47], **SAMOS-2008** [C46], **SAMOS-2009** [C37], **SASP-2009** [C36], **DAC-2010** [C30] and **SASP-2011** [C28]. Among these papers, the **ReSPIR** approach published in **IEEE Trans. on CAD 2009** [J14] represents an innovative approach to apply machine learning to the problem of the efficient design space exploration of multicores. This work represents the first in-depth comprehensive application of the design of experiments (DoE) and response surface modeling (RSM) techniques for the efficient yet accurate multi-objective exploration for multicores. RESPIR introduces an iterative refinement of the Pareto set based on

Response Surface Modeling techniques to analytically model the system behavior in application-specific DSE. The ReSPIR paper was published in 2009 and received up to now **96** citations (according to Google Scholar). I was also **Co-editor** of the scientific book: "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Springer, 2011 [B4].

As follow up, I opened two research paths on design space exploration. The first path is focused on speeding up the DSE phase by introducing predictive simulation scheduling - published at **DATE-2014** [C14] and extended in **IEEE Transactions on CAD 2015** [J5]. The second path is going towards the optimisation of the **high-level synthesis** process by exploiting Response Surface Models to analytically represent an HLS engine. We propose the construction of delay and area RSM models to capture the behavior of the core HLS optimization algorithms (operation scheduling, resource binding and register allocation), enabling the prediction of the design metrics for various data-path configurations resulting from the HLS phase. By adopting the proposed approach, we manage both *(i)* to eliminate the iterative resorting to the costly architectural synthesis procedures, thus accelerating exploration and *(ii)* to explore the HLS design space in a global manner. Recently, RSMs have been used in the field of platform-based design to model processor architectures for reducing simulation time. Within this research work, we differentiate from the aforementioned approaches, since we are applying RSM to model and predict the behavior of HLS optimization algorithms rather than a specific processor architecture. The proposed SPIRIT approach has been published at **DATE-2013** [C19] and extended in **IEEE Transactions on CAD 2015** [J6].

2.1.4. Application Autotuning and Runtime Management for Manycore Architectures

In the era of manycore architectures, effective DSE techniques should not only deal with the hardware design space, but also the software design space: HW/SW co-exploration should support the HW/SW co-design and the runtime adaptability based on the runtime monitoring and management of system resources to guarantee Quality of Service requirements. The main challenge consists of runtime management policies and mechanisms to adapt resource allocation to workload evolution to meet performance and energy efficiency. The research challenge consists of exploiting system resources both at *design-time* and *runtime* based on an efficient design space exploration and customisation methodology. Based on the knowledge on the *design-time* multi-objective exploration, my research path evolved towards the definition of a *runtime* methodology to optimize the allocation and scheduling of different application tasks on the underlying resources of the target manycore architecture.

In 2007, to address this problem in the context of the **MULTICUBE** Project, I started to collaborate with **IMEC** researchers and Giovanni Mariani (at that time, Ph.D. student at University of Lugano, CH). The main contribution of this research was on the exploitation of the synergy of design-time and runtime techniques to get an effective approach towards a power-aware adaptive computing. The results of the design-time exploration are then used at *runtime* to decide how system resources should be allocated to different application tasks running on the manycore system. Running multiple applications while optimizing the Quality of Service on embedded multi/multicore platforms is a huge challenge. Moreover, applications exhibit unpredictable changes of the environment and workload conditions, which makes the task of running them optimally even more difficult. Our research proposes an approach where applications include service routines to dynamically monitor the usage of system resources in manycore architectures. This information is sent to a lightweight Runtime Resource Manager (RRM) to decide the configuration of parameters to be loaded at runtime for each application. This decision is taken dynamically by considering the available platform resources and the application requirements.

Research on runtime resource management techniques has continued in the context of the **FP7-ICT-2009-Call4 2PARMA** European project under my scientific coordination. During 2PARMA project, the proposed runtime methodology has been applied to several application domains to demonstrate its benefits in industrial contexts, such as the **P2012/STHORM** manycore platform provided by STMicroelectronics. The 2PARMA project ended in March 2013 with an excellent evaluation by the European Commission demonstrating the fulfilment of its objectives and scientific/technical goals. Based on the opinion of the European expert reviewers, the 2PARMA project represented a ***"success story"*** and made significant contributions to the state-of-the-art in the field.

Main achievements: The main contribution of my research on adaptivity and runtime management techniques have been published in **DATE-2010** [C31], **DATE-2012** [C24] and more recently in **ARC-2014** [C12], **IC-SAMOS-2014** [C10], **ISPA-2014** [C9], **IC-SAMOS-2015** [C6]. Some of the main contributions are published in the journal papers **PARCO-2013** [J9] and **ACM Trans. on Embedded Computing Systems 2013** [J8]. More oriented to the

learning phase, the approaches we proposed in **TECS-2013** [J8] and **IET-2011** [J13] present in detail the off-line phase used for gathering the knowledge needed to filter and then to exploit at runtime application configurations in terms of software knobs, such as code transformations **DAES-2017** [J18].

In this period, I also started working together with Edoardo Paone (Ph.D. student at Politecnico di Milano) focusing on customisation and optimisation of OpenCL applications for the efficient task mapping under heterogeneous platform constraints. The lack of autotuning and runtime adaptation capabilities at the application level tends to lead to sub-optimal power/performance tradeoffs at the system-level due to the underutilisation of the resources in a manycore architecture. The proposed approach borrows some concepts derived from the approximate and adaptive computing area to give to the application some autotuning capabilities. The system-wide adaptive approach is based on global monitoring, adaptation and optimization. In **ASAP-2014** [C11] and **CODES-ISSS-2012** [C22], the autotuning of OpenCL applications have been investigated and implemented under adaptive resource constraints for manycore architectures.

Another relevant result achieved in collaboration with Edoardo Paone have been published in **DATE-2015** [C7], where the focus has been moved to the application autotuning and mapping based on the **heterogeneous** nature of the underlying platforms. Appropriate self-adaptive techniques are provided to dynamically support migration of code and data among cores. My interest towards **heterogeneous architectures** is motivated by the fact that traditional homogeneous manycores do not represent the best fit to deal with the variety of parallel applications requested by the consumer products. In contrast, heterogeneous systems have shown great potential for performance improvement by introducing specialised cores and accelerators. Heterogeneous manycore systems are considered the most promising computing architecture to cope with power/performance tradeoffs in various domains from embedded to high performance computing. However, core **heterogeneity**, combining general-purpose processor cores with application-specific accelerators, further increase the degrees of freedom in the exploration phase. To exploit the capabilities of heterogeneous architectures, an integrated design and implementation tool chain is required to automatically explore the multi-dimensional design space and optimize the partitioning and mapping to maximize the performance while meeting the given Quality of Service constraints. Research on DSE for heterogeneous multi-core designs will represent a challenging task, i.e. selecting the optimal types and number of system resources in the heterogeneous multi-core for the target workload. Moreover, enabling accelerator-centric architectures is another challenging task. The idea is to provide a design framework to ease the development of accelerators and related programming languages and compiler toolchain and automated tools to exploit their potential computation capabilities. In the context of heterogeneous architectures, we can devise support for code and data migration between different types of processing cores, thus capable to adapt to several processor architectures and hardware accelerators. Joint research with the **Technical University of Delft (NL)** was focused on runtime optimization techniques of dynamically reconfigurable systems. The most relevant results have been published in **FPL-2013** [C18] and **ASP-DAC-2014** [C15]. I believe there are still significant paths dealing with heterogeneity in the era of manycores based on accelerator-centric architectures and dynamic task mapping.

2.1.5. Manycore Architectures based on Networks-on-Chip

Given the increasing complexity of manycore architectures, the current trends on on-chip communication are converging towards the Network-on-Chip (NoC) approach, representing a high bandwidth and low-energy solution. The NoC-based design approach offers several other advantages, such as scalability, reliability, IP reusability and separation of IP design from on-chip communication design and interfacing. NoC design represents a new paradigm to design multi/manycores shifting the design methodologies from a computation-based to a communication-based approach. To address NoC research challenges, I started a new path of my research in 2003 focusing on the topic of low-power NoC for embedded architectures, covering energy-aware design and techniques from several perspectives and abstraction levels. My research on NoC started as advisor of Gianluca Palermo (at that time Ph.D. student at Politecnico di Milano) focusing on the development of **PIRATE,** a modular and flexible framework for power/performance exploration of Network-on-Chip architectures. The PIRATE framework has then been applied to explore distributed shared memory architectures based on NoCs. For this class of systems, I also started a new research path to investigate the problem of synchronization mechanisms and memory management techniques. Most of my research on low-power NoC for embedded architectures have been carried out in the context of two industrial research projects funded by **STMicroelectronics.** I was **Principal investigator** of both research projects, namely: *"Low Power*

Network on Chip and Embedded Architectures" (2003-2005) and *"Low Power Network on Chip and Multiprocessor Platforms" (2006-2008)*. Then my research moved towards the problem of application mapping, optimization and topology customization for the **Spidergon NoC** architecture provided by **STMicroelectronics** (Grenoble, F) in the context of the **MEDEA+ LoMoSA+** project in collaboration with **ALaRI Research Institute** at the University of Lugano (CH).

Main achievements: Main research achievement of my early research on NoC are: *(i)* the development of **PIRATE** framework for NoC optimization (presented in **PATMOS-2004** [C60]) and *(ii)* the development of **GRAPES** modeling and simulation framework for multi-processor Systems-on-Chip based on NoC presented at **IC-SAMOS-2006** [C56] and extended in **JSA-2007** [J17].

One of the most significant results of the research team I was leading at that time at Politecnico di Milano (and composed of Matteo Monchiero, Gianluca Palermo and Oreste Villa) was the definition of ***synchronization techniques*** for distributed shared memory multicore architectures based on Network-on-Chip. The proposed solution is based on the idea of locally performing synchronization operations requiring continuous polling of a shared variable, thus, featuring large contentions (e.g., spin locks and barriers). A hardware (HW) module, the synchronization-operation buffer (SB), has been introduced to queue and to manage the requests issued by the processors. By using this mechanism, we propose a spin lock implementation requiring a constant number of network transactions and memory accesses per lock acquisition. The SB also supports an efficient implementation of barriers. The proposed synchronization techniques appeared in high-impact venues: **DATE-2006** [C57], **ACM SIGARCH-2006** [J20], **IEEE Transactions on VLSI 2006** [J19] and then **CASES-2008** [C42].

In that period, I also started co-advising with prof. Donatella Sciuto the Ph.D. student Giovanni Beltrame on modeling, simulation, analysis and optimization of Multi-Processor System-on-Chip platforms. My contribution was mainly to support the Network-on-Chip modeling and exploration. The target platform has been configured to simulate an IPv4 forwarder based on the StepNP framework (developed at STMicroelectronics Research Labs, Ottawa) applied to an MPEG4 VGA encoder and an Ogg-Vorbis encoder. These applications have been modeled by introducing a multi-accuracy transaction-level approach, then explored and optimized in terms of power and performance.

The **main outcomes** of the research done in collaboration with prof. Donatella Sciuto and Giovanni Beltrame have been published in the proceedings of top-level conferences (**CASES-2004** [C59], **DATE-2006** [C58] and **CODES-ISSS-06** [C54]) then extended in the **IEEE Trans. on CAD 2007** [J16].

In 2007, I started investigating about **security** aspects in NoCs together with Gianluca Palermo and Leandro Fiorin (Ph.D. student at University of Lugano, CH). Our seminal work appeared at **CODES-ISSS 2007** [C50] still remains to this day one of the first approaches to investigate an important, but unaddressed aspects of NoCs, namely ***security.*** The work was extended in the prestigious **IEEE Trans. on Computers 2008** [J15]. In this paper, we present a secure NoC architecture composed of a set of Data Protection Units (DPUs) implemented within the Network Interfaces (NIs). The runtime configuration of the programmable part of the DPUs is managed by a central unit, the Network Security Manager (NSM). The DPU, similar to a firewall, can check and limit the access rights (none, read, write, or both) of processors accessing data and instructions in a shared memory. In particular, the DPU can distinguish between the operating roles (supervisor/user and secure/nonsecure) of the processing elements. We explore alternative implementations of the DPU and demonstrate how this unit does not affect the network latency if the memory request has the appropriate rights. We also focus on the dynamic updating of the DPUs to support their utilization in dynamic environments and on the utilization of authentication techniques to increase the level of security. Our work on the programmable data protection device and secure programming manager has been the subject of one **European patent application [P5-EU]** in collaboration with **STMicroelectronics** extended to one **US Patent granted in 2012 [P5-US].**

Afterwards, we opened a new research path by adding **high-level services** and **runtime monitoring** on top of the standard communication services usually provided by NoCs. In this work, we propose to monitor runtime system activities in adaptive NoC-based manycore platforms through the observation of transactions performed on the communication subsystem. As central element of architectures based on the communication-centric paradigm, NoCs are the ideal mean to collect information about cores, and more general system behavior. Being the NoC the central component in multi/many architectures, it can be used as an element to observe and control the global system activity in a way transparent to processing and storage cores, as well as to provide high-level services that can be executed in parallel to protocol translation and data transmission. Three types of services have been addressed and discussed: security, runtime monitoring, and fault detection

and fault tolerance.

Main achievements: Secure monitoring services for NoCs have been presented in **CODES-ISSS-2008** [C40], while a runtime monitoring system based on NoCs has been proposed in **DATE-2009** [C38] and extended in the **IEEE Trans. on VLSI-2014** [J7]. Finally, I was also **Co-editor** of the scientific book: *"Low-Power Networks-on-Chip"* published by Springer in 2011 [B3].

Moreover, joint research has been carried out in collaboration with the **Universidade Federal do Rio Grande do Sul** in Porto Alegre (Brasil) focusing on floor planning-aware exploration for application-specific NoC and adaptive buffers for virtual channel routers in NoCs. In this research, we focus on floorplanning-aware exploration for application-specific hierarchical NoCs. In this work, we propose HASIN – Hierarchical Adaptive Switching Interconnection Network, an architecture that explores the suitable switching architecture according to the bandwidth requirements for each region of a system, in a hierarchical manner **ISCAS-2012** [C23], **NoCArc-2011**[C26] and **VLSI-SoC-2011** [C27]. The proposed interconnection adapts the network at runtime by using three switching possibilities and for this, it uses floorplan information to reconfigure itself. The adaptability at the system-level is required due to some unforeseen situations at design time. In these cases, we can consider the possibility of updates in the system with changes in the communications rates, the fact that the traffic does not present a constant behavior, as the occurrence of burst or still the reason that is not possible to integrate all cores with high communication in the same cluster due the restrictions of the crossbar size.

2.1.6. Technology-aware Manycore Architectures Design

A basic tenet of my research is that low power application-specific manycore architectures must be tuned being aware of microarchitectural and technology problems and emphasizing the early-phase of design space exploration. Many challenging and relevant research topics related to manycore architectures are still open. There is still significant research to be done, and architectural and technology challenges will increase in importance as we scale down the fabrication process in the nanoscale era. I believe that technology-driven considerations (such as ultra-low-power design, resiliency and process variability) will further increase their importance on architecture and system level design in the next coming years. In the manycore era, system design optimization and exploration still represent challenging tasks. Networks-on-Chip, as an architectural solution for scalable high-speed interconnect, and power-aware design will continue to be crucial topics, since power and energy issues still represent one of the limiting factors in integrating multi/manycores on a single chip. The power-wall problem and its dual utilization-wall problem are considered among the main barriers for an efficient performance scaling bringing to the **dark silicon** problem (where for dark silicon is intended the chip fraction not usable in a manycore chip due to the power budget). To address the dark silicon problem, **Near Threshold Computing (NTC)** has recently been proposed as a promising solution to mitigate the dark silicon effects by operating at lower frequency but exploiting a larger number of cores. However, NTC suffers from an increase sensitivity to technology problems (such as process variability). In this context, in 2011, I opened a new research path in collaboration with Gianluca Palermo and Sotirios Xydis (currently Post-doc at the National Technical University of Athens, formerly Post-doc at POLIMI) and Ioannis Stamelakos (at that time Ph.D. student at POLIMI). The main focus of our research was on **variability-aware NTC** architectures based on the formation of voltage islands with emphasis on voltage and workload allocation across the manycore architecture. We also introduced the usage of approximate computing concepts to sustain performance despite of variability effects.

Main achievements: Our former research works on variability-aware robust DSE for manycore architectures have been published in **ASP-DAC-2009** [C39] and in **ACM Trans. on Embedded Computing Systems 2012** [J11]. Our most recent achievement consists of a variability-aware framework based on fine-grained voltage islands for exploring the potential power-efficiency of NTC under performance constraints. The proposed approach has been presented in high-impact venues: **ASP-DAC 2014** [C15], **DATE 2014** [C14] and more recently in **ISVLSI-2016** [C3] and **PATMOS-2016** [C2]. Finally, I was also **Co-editor** of the scientific book titled: **"Near Threshold Computing"** published by Springer in 2015 [B2].

2.2. ON-GOING RESEARCH DIRECTIONS

The research experience gained on design space exploration and runtime resource management for manycore architectures lead me towards one of my recently opened research paths: **Application Autotuning for High Performance Computing.** This research path represents the core concept I have proposed as Scientific Coordinator in the **H2020 ANTAREX** research proposal, accepted for funding under the competitive H2020-FET-HPC Call 1 held in 2014. The acceptance rate of the call was **23 %** (19 RIA proposals accepted out of 83 submitted). The ANTAREX grant provides globally **3.1 Meuro** for a Consortium with eight partners including top-ranked universities, two supercomputing centers and two industrial application providers. The main goal of the project is to provide a breakthrough approach to express by a Domain Specific Language the application self-adaptivity and to runtime manage and autotune applications for energy-efficient HPC systems.

2.2.1. *Application Autotuning for High Performance Computing*

Designing and tuning applications for energy-efficient High Performance Computing systems up to the Exascale era is an extremely challenging problem. Exascale supercomputers (reaching billions of billions floating point operations per second) cannot be built by simply expanding the number of processing nodes and leveraging technology scaling, as power demand would increase unsustainably (up to hundreds of MW). To reach the DARPA[2]'s target of 20MW of Exascale supercomputers projected to the year 2020, current supercomputers (reaching up to 93 PetaFlop/s) must achieve an energy efficiency "quantum leap". The Green500 list looks at the GigaFlops per Watt as energy efficiency metric to rank supercomputers by their energy efficiency. According to the latest Green500 list published in November 2017, the "most green" supercomputers are all occupied by heterogeneous systems (based on accelerator/co-processor technology) equipped with Intel Xeon processors and NVIDIA's Tesla P100 GPUs. Next generation of green HPC heterogeneous systems will integrate the latest NVIDIA Volta GV100 GPU to further accelerating the computation. The dominance of heterogeneous systems in the Green500 list is expected to continue for the next coming years to reach the target of 20MW Exascale supercomputers. *However, to fulfil the Exascale target, energy-efficient supercomputers need to be coupled with a radically new software stack capable of exploiting the benefits offered by architecture heterogeneity at different abstraction levels to meet the scalability and energy efficiency required by the Exascale era.*

The automatic application customization and optimization (also called *autotuning,* or *self-adaptability* if done at runtime) has emerged as a key technique for enabling High Performance Computing by adjusting the application behavior in the face of changing operating conditions and resource availability. In spite of the application-independence, recent approaches in literature mainly rely on loop-level knobs in the code and on a predictable execution context. Autotuning is beneficial in guaranteeing performance portability of a program across heterogeneous resources, while responding to the dynamic evolution of non-functional requirements, typically represented by conflicting metrics such as energy and delay. System adaptivity needs to be scaled dynamically in an autonomic way, optimizing the large-scale computing capabilities with respect to dynamically changing workloads, computational demands, resource availability while meeting the application requirements on power budget and Service Level Agreement (SLA). *So far, there are not yet any adequate programming model and toolchain to develop, deploy and maintain HPC applications, which exhibit the required high-levels of portability, dynamicity and context-aware behavior.*

One key innovation of the ANTAREX approach consists of introducing a separation of concerns (where self-adaptivity and energy efficient strategies are specified aside to application functionalities) promoted by the definition of a Domain Specific Language (DSL) inspired by aspect-oriented programming concepts for heterogeneous systems. The new DSL is introduced for expressing at compile time the adaptivity/energy/performance strategies, languages, methodologies and tools and to enforce at runtime application autotuning and resource and power management. The goal is to support the parallelism, scalability and adaptability of a dynamic workload by exploiting the full system capabilities (including energy management) for emerging large-scale and extreme-scale systems, while reducing the Total Cost of Ownership (TCO) for companies and public organizations. ANTAREX approach is based on:

- introducing a new DSL for expressing adaptivity and autotuning strategies;
- enabling the performance/energy control capabilities by introducing software knobs (including application parameters, code transformations and code variants);

[2] Defense Advanced Research Projects Agency (DARPA) of the U.S. Department of Defense

- designing scalable and hierarchical optimal control-loops capable of dynamically leveraging them together with performance/energy control knobs at different time scale (compile time, deployment time and runtime) to always operate the supercomputer and each application at the maximum energy-efficient and thermally-safe point.

This is done by monitoring the evolution of the HW supercomputer as well as the application status and requirements and bringing this information to the ANTAREX energy/performance-aware software stack. The ANTAREX project is on-going and driven by industrial two use cases, chosen to address the self-adaptivity and scalability characteristics of **two** highly relevant HPC application scenarios. These two use cases have been selected due to their significance in emerging application trends and thus by their direct economic exploitability and relevant social impact:

1. A biopharmaceutical HPC application provided by Dompé for accelerating drug discovery deployed on the Marconi Tier-0 Intel-based system based at CINECA (Marconi is currently ranked at the 14th position of the Top500 list and it is the second most powerful supercomputer in Europe);
2. A self-adaptive navigation system provided by Sygic to be used in smart cities deployed on the server-side on a heterogeneous Intel-based PetaFlops class system provided by IT4Innovations Supercomputing Center.

All the key ANTAREX software innovation are designed to scaled-up to the Exascale level. Performance metrics extracted from the two use cases are modelled to extrapolate these results towards Exascale systems.

ANTAREX project started in September 2015 for a 3-year duration. As ANTAREX Project Coordinator, I have presented the seminal research concepts of the ANTAREX project at **EUC-2015** [IP2], **CF-2016** [C4] and **DATE-2016** [C5]. With the ANTAREX funding received at Politecnico di Milano, I have formed a research group in collaboration with my colleague prof. Gianluca Palermo and we hired two PhD students and one post-doc researcher in the fall 2015. These students developed the first prototype of the open-source **mARGOt autotuner**[3], demonstrated to EC technical experts in May 2017. Starting from the idea of non-domain knowledge, mARGOt can be fed by code annotations to shrink the search space by focusing the autotuner on a certain subspace. The framework includes a monitoring loop used to monitor the application and to trigger the application adaptation. The monitoring, together with application properties/features, represents the main support to the decision-making during the application auto-tuning phase since it will be used to perform statistical analysis related to system performance and other Service Level Agreemwnt aspects. Continuous on-line learning techniques enable to update the knowledge from data collected by the monitors, giving the possibility to autotune the system according to the more recent operating conditions. Machine learning techniques, such as neural networks and decision trees, are used in the decision-making engine to support the autotuning by predicting the most promising set of parameter settings. The LARA-based DSL is used to express code variants (i.e. different implementations of the same computation) and application parameters, in terms of discrete set of values to govern code generation and execution of a single code variant. Thus, the ANTAREX approach will export the application knobs “out of the box” for being managed by the mARGOt autotuning framework.

As Scientific Coordinator of ANTAREX, I also maturated very fruitful research collaborations with the group of prof. Joao Cardoso at University of Porto on the LARA DSL and the group of prof. Luca Benini at ETH Zurich on the open-source Examon scalable framework for performance and energy monitoring of HPC systems. The work developed in collaboration with University of Porto -- recently accepted for publication in **DATE-2018** [C1] -- introduces a structured approach, called **SOCRATES,** for the runtime selection of the most suitable application configuration in terms of compiler flags and parallelism parameters of the OpenMP runtime. The main contribution of SOCRATES is to offer runtime autotuning features, while avoiding any manual intervention by the application developer. SOCRATES uses the LARA aspect-oriented language to implement the separation of concerns between the functional and extra-functional parts of the application, while an application-level autotuner, mARGOt is integrated for the optimal configuration selection. All changes to the application code required by SOCRATES are automatically done by LARA. Furthermore, SOCRATES supports an energy efficient execution by introducing energy consumption as a key variable to be considered at runtime.

[3] https://gitlab.com/margot_project

2.2.2. Compiler Autotuning based on Machine Learning

In the context of ANTAREX, I also started my research on **compiler autotuning based on machine learning techniques** to speed up application performance and to reduce the cost of compiler optimization phases. The most significant contributions on compiler autotuning based on the introduction of Bayesian networks led to the **COBAYN** framework that has been recently published in **TACO-2016** [J4]. **COBAYN** (**CO**mpiler autotuning framework using **BAY**esian **N**etworks) is based on the application characterization done dynamically by using independent microarchitecture features and Bayesian networks. The work has been carried out in collaboration with Amir H. Ashouri (Ph. D. student at POLIMI under my supervision and currently post-doc at the University of Toronto).

So far, researchers have proposed two main approaches for tackling the problem of identifying the best compiler optimizations: (i) iterative compilation and (ii) machine- learning (ML) predictive modeling. The former approach relies on several recompilation phases, then selecting the best set of optimizations. Obviously, this approach—although effective—has high overhead, as it needs to be evaluated iteratively. The latter approach focuses on building ML models to predict the best set of compiler optimizations. It relies on software features that are collected either offline or online. Once the model is trained, given a target application, it can predict a sequence of compiler optimization options to maximize performance. ML approaches need fewer compilation tryouts. There is a downside, however: typically, the performance of the final execution binary, which is worse than the one found with iterative compilation.

In COBAYN, we propose to tackle the problem of identifying the compiler optimizations that maximize the performance of a target application. In contrast to prior work, the COBAYN approach starts by applying a statistical methodology to infer the probability distribution of the compiler optimizations to be enabled. Then, it starts to drive the iterative compilation process by sampling from this probability distribution. Two major sets of training application suites are used to learn the statistical relations between application features and compiler optimizations. In COBAYN, Bayesian Networks are used for the first time in this field to build the statistical model. Given a new application, its features are fed into the ML algorithm as evidence on the distribution. This evidence imposes a bias on the distribution; because compiler optimizations are correlated with the software features, we can iteratively sample the distribution, obtaining the most promising compiler optimizations by then exploiting an iterative compilation process.

The experiments carried out on an embedded ARM-based platform outperformed both standard optimization levels and the state-of-the-art iterative and not iterative (based on prediction models) compilation techniques, while using the same number of evaluations. Moreover, the proposed techniques demonstrated significant exploration efficiency improvement of up to 4× speedup compared with random iterative compilation when targeting the same performance.

COBAYN addresses the hard problem of the selection of the right set of compiler optimizations for a particular code segment, however finding the best ordering of these optimizations adds further complexity. Finding the best ordering represents a long standing problem in compilation research, named the **phase-ordering problem.** Traditional approaches based on constructing compiler heuristics to solve this problem cannot cope with the enormous complexity of choosing the right ordering of optimizations for every code segment in an application. Continuing my collaboration with Amir Ashouri, we recently proposed an automatic optimization framework, namely **MiCOMP,** to **Mi**tigate the **Com**piler **P**hase-ordering problem based on the optimization of sub-sequences and machine learning. The work has been recently published in **TACO-2017** [J2].

MiCOMP performs phase ordering of the optimizations in LLVM's highest optimization level using optimization sub-sequences and machine learning. The idea is to cluster the optimization passes of LLVM's O3 setting into different clusters to predict the speedup of a complete sequence of all the optimization clusters instead of having to deal with the ordering of more than 60 different individual optimizations. The predictive model uses (1) dynamic features, (2) an encoded version of the compiler sequence, and (3) an exploration heuristic to tackle the problem. Experimental results by using the LLVM compiler framework and the Cbench suite show the effectiveness of the proposed clustering and encoding techniques to application-based reordering of passes, while using a number of predictive models. We perform statistical analysis on the results and compare against (1) random iterative compilation, (2) standard optimization levels, and (3) two recent prediction approaches. We show that MiCOMP's iterative compilation using its sub-sequences can reach an average performance speedup of 1.31 (up to 1.51). Additionally, we demonstrated in **TACO-2017** [J2] that MiCOMP's prediction model outperforms the -O1, -O2, and -O3 optimization levels within using just a few predictions and reduces

the prediction error rate down to only 5%. Overall, it achieves 90% of the available speedup by exploring less than 0.001% of the optimization space.
Finally, a collection of the most significant contributions of my research group on **compiler autotuning** has been recently published in the Springer book: "Automatic Tuning of Compilers using Machine Learning" [B1]. An heustaustive survey on compiler autotuning using machine learning has been recently accepted for publication by the **ACM Computing Surveys** [J1].

2.3. RESEARCH COLLABORATIONS

My research activities have been done in collaboration with several national and international universities, research centers and several ICT and semiconductor companies. Among them, we can mention (in chronological order):

1. **STMicroelectronics** - Agrate, Italy (1996 - Present), Contact Person: Dr. R. Zafalon. Research topics: Power estimation and optimization techniques for Network on-Chip architectures (1996 – 2006); Design space exploration of embedded computing architectures (2007 – 2010).
2. **ALaRI** - Advanced Learning and Research Institute - Switzerland (2003 - Present), Contact Person: prof. M. Sami. Research topics: Design space exploration techniques based on response surface methods. Design and analysis of high-level services for Network on-Chip architectures.
3. **IMEC** - Interuniversity Micro-Electronics Centre, Belgium (2007 - 2013), Contact Persons: prof. Francky Catthor, Chantal Ykman Couvreur, Research topic: Design and analysis of an application-specific manager for power-aware adaptation.
4. **STMicroelectronics** - Grenoble, France (2005 - 2007), Contact Person: Dr. M. Coppola. Research topic: Design methodology and implementation of high-level services on the ST-NOC architecture.
5. **STMicroelectronics** - Grenoble, France (2010 - 2013), Contact Person: Dr. D. Melpignano. Research topic: Design methodology and tools for manycores computing fabrics.
6. **Fraunhofer - Heinrich Hertz Institut** – Berlin, Germany (2010 – 2013), Contact Person: Dr. Benno Stabernack. Research topics: Design space exploration od Scalable Video Coding applications
7. **NTUA** - National Technical University of Athens - Greece (2010 - Present), Contact Persons: prof. D. Soudris, Dr. S. Xydis. Research topics: Runtime management techniques for manycore architectures; Design and exploration of Near-Threshold Computing architectures.
8. **TUDelft** – Technical University Delft, The Nederlands (2008 - 2013), Contact Person: prof. K. Bertels. Research topics: Design space exploration and runtime management techniques for reconfigurable computing platforms.
9. **PNNL** - Pacific Northwestern National Laboratory - WA, USA (2010 - Present), Contact Persons: Dr. A. Tumeo, Dr. O. Villa (currently at NVIDIA). Research topics: Design and analysis of a manycore/many-node architecture for irregular applications.
10. **UFRGS** - Universidade Federal do Rio Grande do Sul - Brazil (2009-2011), Contact Person: prof. L. Carro Research topic: Floorplan-aware design methodology for Network on-Chip architectures.
11. **IBM Research** - ASTRON & IBM Center for Exascale Technology, The Nederlands (2013 – Present), Contact Persons: Dr. L. Fiorin and Dr. G. Mariani. Research topic: Architectures and applications for exascale computing.
12. **UCI** - University of California at Irvine – CA, USA (2013 – 2016) Contact Person: prof. Fadi Kurdahi. Research Topic: Near Threshold Computing for manycore architectures.
13. **University of Delaware, USA** (2014 – 2017), Contact Person: prof. John Cavazos. Research Topic: Machine learning techniques for compiler optimization.
14. **STMicroelectronics** – Castelletto di Settimo Milanese, Italy (2014 - Present), Contact Person: Dr. G. Desoli. Research topic: Design methodology and tools for Deep Convolutional Neural Networks.
15. **CINECA, Italy** (2015 – Present), Contact Person: Dr. Carlo Cavazzoni and Dr. Nico Sanna. Research Topic: Energy-efficient High Performance Computing systems.
16. **Universidade do Porto, Portugal** (2015 – Present), Contact Person: Prof. Joao Cardoso. Research Topic: Application and compiler autotuning based on Domain Specific Languages
17. **ETH Zurich, Switzerland** (2015 – Present), Contact Person: Prof. Luca Benini. Research Topic: Energy-

efficient High Performance Computing.

2.4. *RESEARCH COLLABORATORS/CO-AUTHORS/CO-EDITORS*

- My research activities have been done in collaboration with several national and international collaborators/co-authors/co-editors with external affiliation. About **100** out of **160** scientific publications include co-authors with different affiliations (**50** out of them are industrial co-authors, **150** co-authors overall). Among them, let me mention (in alphabetical order):

  Gerd Ascheid (Aachen University, Germany), Prabhat Avasare (IMEC, Belgium), Andrea Bartolini (ETHZ, Switzerland), Sanzio Bassini (CINECA, Italy), Alex Bartzas (EXUS, Greece), Andrea Beccari (Dompé, Italia), Luca Benini (ETHZ, Switzerland), Mladen Berekovic (TU Braunschweig, Germany), Koen Bertels (Delft Technical University, The Nederlands), Sara Bocchio (STMicroelectronics, Italy), Umberto Bondi (University of Lugano, Switzerland), Jens Brandenburg (Fraunhofer HHI, Germany), João Cardoso, (University of Porto, Portugal), Luigi Carro (UFRGS, Brazil), Jeronimo Castrillon (Dresden Technical University, Germany), Franky Catthoor (IMEC, Belgium), John Cavazos (University of Delaware, USA), Carlo Cavazzoni (CINECA, Italy), Peter Cheung (Imperial College London, UK), Radim Cmar (Sygic, Slovakia), Caroline Concatto (UERGS, Brazil), Marcello Coppola (STMicroelectronics, France), Giovanni De Micheli (EPFL, Switzerland), Giuseppe Desoli (STMicroelectronics, Italy), Giovanni Erbacci (CINECA, Italy), Dongrui Fan (ICT - Chinese Academy of Sciences, China), Leandro Fiorin (IBM-ASTRON, The Nederlands), Franco Fummi (University of Verona, Italy), Arpad Gellert (Sibiu University, Romania), Carlo Guardiani (STMicroelectronics, Italy), Paolo Gubian (University of Brescia, Italy), Zhang Hao (ICT - Chinese Academy of Sciences, China), Michael Huebner (Ruhr Universitaat Bochum, Germany), Carlos Kavka (ESTECO, Italy), Torsten Kempf (Cognex Corporation, Germany), Fadi Kurdahi (University of California at Irvine, USA), Marcello Lajolo (NEC Labs, USA), Rainer Leupers (Aachen University, Germany), Wayne Luk (Imperial College London, UK), Enrico Macii (Politecnico di Torino, Italy), Giovanni Mariani (IBM-ASTRON, The Nederlands), Marco Martinez (DS2, Spain), Jan Martinovic (IT4Innovations, Czech Republic), Debora Matos (UERGS, Brazil), Diego Melpignano (STMicroelectronics, Italy), Smail Niar (University of Valenciennes, France), Luca Onesti (ESTECO, Italy), Martin Palkovic (IT4Innovations, Czech Republic), Pierre Paulin (Synopsys, Canada), Hector Posadas (University of Cantabria, Spain), Erven Rohou (INRIA, France), Ingo Sander (KTH, Sweden), Nico Sanna (CINECA, Italy), Michael Schulte (AMD, USA), Vlad-Mihai Sima (Bluebee, The Nederlands), Katerina Slaninova (IT4Innovations, Czech Republic), Dimitrios Soudris (National Technical University of Athens, Greece), Benno Stabernack (Fraunhofer HHI, Germany), Giulio Urlini (STMicroelectronics, Italy), Geert Vanmeerbeeck (IMEC, Belgium), Eugenio Villar (University of Cantabria, Spain), Lucian Vintan (Sibiu University, Romania), Vit Vondrak (IT4Innovations, Czech Republic), Marise Wouters (IMEC, Belgium), Sotirios Xydis (National Technical University of Athens, Greece), Chantal Ykman-Couvreur (IMEC, Belgium), Roberto Zafalon (STMicroelectronics, Italy)

2.5. *COORDINATION OF EUROPEAN RESEARCH PROJECTS*

- **Project Coordinator of the H2020-FET-HPC European Project ANTAREX-671623** on "AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems" (Sep. 2015 - Aug. 2018). www.antarex-project.eu. The project won a **3.1 M€ grant** in the H2020 Future and Emerging Technologies programme on High Performance Computing in 2015. **The acceptance rate of the FET-HPC-2014 Call 1 was 23 %** (19 RIA proposals accepted out of 83 submitted). The project involves leading academic and industrial partners as well as CINECA, the Italian Tier-0 supercomputing centre and IT4i, the Czech Tier-1 supercomputing center. Being one of the nineteen research projects in the **FET-HPC-2014 Call 1,** ANTAREX brings the partners on the forefront of the European research in High Performance Computing. The main goal of the ANTAREX project is to provide a breakthrough approach to express by a Domain Specific Language the application self-adaptivity and to runtime manage and autotune applications for green and heterogeneous High Performance Computing systems up to the Exascale level. The Consortium also includes three top-ranked academic partners (ETH Zurich, University of Porto, and INRIA). Industrial partners include one of the leading biopharmaceutical companies in Europe (Dompé) and the top European navigation software company (Sygic).
- **Project Coordinator of the European Project FP7-2PARMA-248716** on "PARallel PAradigms and Run-time MAnagement techniques for Manycore Architectures" (Jan. 2010 – Mar. 2013). http://www.2parma-project.eu/ EC Contribution to the project: **2.7 M€ funding.** The 2PARMA Consortium was composed of seven partners: Politecnico di Milano (Italy), STMicroelectronics (Italy and France), Heinrich Hertz Institute

- Fraunhofer Institute for Telecommunications (Germany), IMEC (Belgium), ICCS - Institute of Communication and Computer Systems (Greece), RWTH Aachen University (Germany), Synopsys (Belgium). The 2PARMA project focused on the definition of a parallel programming models, runtime resource management policies and design space exploration methodologies for manycore architectures. Applicability and benefits of the proposed techniques and tools have been validated and assessed on as set of industrial applications and hardware platforms. The 2PARMA project ended in March 2013 receiving by the European Commission a final overall rating of "***excellent"*** *(the highest a project can get)* demonstrating the fulfilment of its objectives and scientific/technical goals. The expected impact was also considered excellent. The European experts commended me as Project Coordinator: *"for the efficiency and professionalism shown during the whole project; for demonstrating high management skills and strong leadership abilities and for establishing an efficient and effective collaboration amongst all the project partners".*The 2PARMA project has been selected in 2013 as a ***"success story"*** by the panel of experts from the Directorate-General for Communications, Networks, Content and Technology (DG-CONNECT) of the European Commission: *"for significant contributions to the state-of-the-art in the field".* The 2PARMA project has been presented as one of the success stories during the Conference: "Cyber-Physical Systems: Uplifting Europe's innovation capacity", 29-30 October 2013 in Brussels.

- **Project Coordinator of the European Project FP7-MULTICUBE-216693** on "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (Jan. 2008 - June 2010). http://www.multicube.eu/ EC Contribution to the project: **2.1 M€ funding.** The MULTICUBE Consortium was composed of nine partners: Politecnico di Milano (Italy), Design of Systems on Silicon – DS2 (Spain), STMicroelectronics (Italy), IMEC (Belgium), ESTECO (Italy), University of Lugano - ALaRI (Switzerland), University of Cantabria (Spain), STMicroelectronics Beijing (China), Institute of Computing Technology – Chinese Academy of Sciences (China). The MULTICUBE project finished in 2010 with an ***excellent final overall rating*** based on the opinion of the panel of experts from the Directorate-General DG-CONNECT of the European Commission. The project demonstrated to achieve its scientific/technical goals, in particular the benefits of using automated design exploration techniques (based on enhanced multi-objective optimization) on some industrial use cases; practical ways to trade off accuracy for speed through the use of multi-abstraction level simulation thus enabling exploration of larger design spaces; the feasibility of automated parameter tuning at runtime using exploration data collected at design-time. Based on the opinion of the European experts, as Project Coordinator I have demonstrated "*high leadership capabilities and led very professionally all the management activities".* In the context of the MULTICUBE project, I was also leading a research group at Politecnico di Milano whose research focuses on design space exploration for multi-processor architectures working on an open-source tool **(MULTICUBE Explorer)** to enable an automatic and fast optimization of configurable system architectures towards a set of objective functions such as energy and delay.

2.6. *COORDINATION OF INDUSTRIAL FUNDED RESEARCH PROJECTS*

- **Project Manager** of the **IBM/Politecnico di Milano Collaborative Innovation Center on Big Data Analytics** (2015-Present).
- **Principal Investigator** of the two-year research project: "Low Power Network on Chip and Multiprocessor Platforms" (2006-2008) between the Dipartimento di Elettronica e Informazione of Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics,** Agrate B.
- **Principal Investigator** of the two-year research project: "Low Power Network on Chip and Embedded Architectures" (2003-2005) between the Dipartimento di Elettronica e Informazione of Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics,** Agrate B.

2.7. *PARTICIPATION TO EUROPEAN RESEARCH PROJECTS*

- Participation to the **European Integrated Project CONTREX - 611146** on "Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties" (Oct. 2013 – Sep. 2016). https://contrex.offis.de/home/ EC Contribution to the project: 6 M€. The CONTREX project includes fourteen partners from six countries. Project Coordinator: OFFIS (D). Local Principal Investigator: prof. W. Fornaciari. Project Partners: STMicroelectronics Srl – Italy, GMV Aerospace and Defence – Spain, Cobra Telematics (Switzerland), EuroTech SpA (Italy), Intecs SpA (Italy), iXtronics GmbH (Germany), EDALAB Srl – Italy, Docea Power (France), Politecnico di Milano – Italy, Politecnico di Torino – Italy, Universidad de Cantabria – Spain, Kungliga Tekniska Högskolan (Sweden), ECSI – France.

- Participation to the **European Project FP7-HARPA-612069** on "Harnessing Performance Variability" (Sep. 2013 – Aug. 2016). http://www.harpa-project.eu/ EC Contribution to the project: 2.8 M€. The HARPA project includes eight partners from six countries. Project Coordinator: prof. W. Fornaciari, Politecnico di Milano. Project Partners: IMEC (Belgium), ICCS - Institute of Communication and Computer Systems (Greece), University of Cyprus (Cyprus), IT4Innovations VSB - TECHNICKA UNIVERZITA OSTRAVA (Czech Republic), STMicroelectronics (France), THALES COMMUNICATIONS & SECURITY SAS (France), HENESIS S.R.L. (Italy). The goal of HARPA project is to enable next-generation embedded and high-performance heterogeneous manycores to cost-effectively compare variations by providing dependable-performance: correct functionality and timing guarantees throughout the expected lifetime of a platform under thermal, power, and energy constraints.
- Participation to the **ARTEMIS-2009-1-100230 SMECY Project** on "Smart Multicore Embedded Systems" (Feb. 2010 – Jan. 2013). http://www.smecy.eu The SMECY project includes thirty partners (among them STMicroelectronics and Thales) from nine European countries for a total funding of 19 M€. Project Coordinator: Francois Pacull (CEA Leti, France). Local Principal Investigator: prof. D. Sciuto. The vision of the SMECY consortium is that a holistic approach for the integration of multi-core SoC and embedded software technologies is required. Then, the mission of the project is to develop programming and design methods, multi-core architectural solutions and associated supporting tools enabling the exploitation of many (100s) core architectures. The key outcomes of the SMECY project are programming and design methods, multi-core programmable architectural solutions and associated supporting tools that enable a holistic integration of multi-core SoC design and embedded software to master smart system design of future smart multi-core embedded systems in different applications, e.g. consumer, wireless, communication and transportation.
- Participation to the **European Integrated Project COMPLEX - 247999** on "Co-design and power management in platform-based design space exploration" (Dec. 2009 – Feb. 2013). https://complex.offis.de/ EC Contribution to the project: 4.8 M€. The COMPLEX project included fourteen partners from six countries (including China). Project Coordinator: OFFIS (D). Local Principal Investigator: prof. W. Fornaciari. Project Partners: Thales Communications SA –France, Synopsys Belgium NV – Belgium, Universidad de Cantabria – Spain, EDALAB Srl –Italy, Magillem Design Services SAS – France, STMicroelectronics Srl – Italy, STMicroelectronics (Beijing) – China, GMV Aerospace and Defence – Spain, Politecnico di Milano – Italy, Politecnico di Torino – Italy, Chipvision Design Systems– Germany, IMEC – Belgium, ECSI – France. Rising heterogeneity and complexity of embedded systems results into gaps and defines challenges that a leading industry has to face. such as handling complexity of execution platforms and applications, uncertainty of platform selection and application to platform mapping, balancing between increasing power consumption, performance, and explicit application needs and meeting memory demands both in size and access times. The primary objective of COMPLEX is to develop an innovative, highly efficient and productive design methodology and a holistic framework for iteratively exploring the design space of embedded hardware/software (HW/SW) systems.
- From 2006 to 2007, I collaborated as **Senior Researcher** with ALaRI-Advanced Learning and Research Institute, part of the Faculty of Informatics of the Università della Svizzera Italiana (USI) to the European research project **MEDEA+ LoMoSA+** (2A708): "Low-power expertise for Mobile & multi-media System Applications". Project Coordinator: NXP Semiconductors (NL). Local Principal Investigator: prof. M. Sami. The activity carried out in this project has been the subject of one European **patent application** [P5-EU], afterwards extended to the USA (**US patent** [P5-US] granted in 2012). Project partners: STMicroelectronics, Thales, Thomson, DS2, CEA-LETI, CEA-LIST, TIMA, ALaRI, University of Cantabria. Our research activity on a definition of a secure Network-on-Chip architecture has been done in collaboration with STMicroelectronics (Grenoble, F).
- Participation to the **European Project MEDEA+(A207) Pocket Multimedia** "Silicon application platform for pocket multimedia" (2001 – 2004). Project Coordinator: ST Microelectronics. Local Principal Investigator: Roberto Zafalon. In 2005, the project has won the annual award for European collaborative innovation in Microelectronics, the "Jean-Pierre Noblanc Award for Excellence."
- Participation to the **European Project FP6 - ICODES – 004452** "Interface and communication based design of embedded systems" (2004-2007). Project coordinator: OFFIS (D). Local Principal Investigator: prof. D. Sciuto. Project Coordinator), Magillem Design Services (F), Nokia Siemens Networks (I), Robert Bosch (D),

European Electronic Chips & Systems Design Initiative (F), Thales Communications (F), Politecnico di Milano (I).

- Participation to the **European Project FP6 – PEOPLE - 26796** "Power EstimatiOn for fast exPLoration of Embedded systems" funded by ESPRIT4-OMI (Open Microprocessor Initiative) from 1/4/1998 to 31/12/2000. Project coordinator: OFFIS (D). Local Principal Investigator: prof. D. Sciuto. Project partners: Alcatel, ARM, Italtel, LEDA (Languages for Design Automation), OFFIS-University of Oldenburg (Project Coordinator) and Politecnico di Torino-CEFRIEL.

2.8. PARTICIPATION TO NATIONAL RESEARCH PROJECTS

- Two-year scientific national inter-university co-funded research program **MIUR – PRIN 2005** (Prot. 2005095528) "Metodologie di progettazione di sistemi multiprocessore on-chip basati sul concetto di piattaforma" (Design methodologies of multiprocessor systems-on-chip based on the concept of platform). National Scientific Coordinator: prof. D. Sciuto (Politecnico di Milano). Project Partners: Politecnico di Milano, Politecnico di Torino, Università degli Studi di Bologna, Università degli Studi di Catania, Università degli Studi di Verona.
- Two-year scientific national inter-university co-funded research program **MIUR–2002** (Prot. 2002092153) "Metodologie di progetto per sistemi digitali integrati su singolo chip di tipo embedded" (Design methodologies for single-chip embedded systems). National Scientific Coordinator: prof. M. Sami (Politecnico di Milano) Project Partners: Politecnico di Milano, Università degli Studi di Bologna, Università degli Studi di Urbino "Carlo Bo", Università degli Studi di Catania, Università degli Studi di Verona, Politecnico di Torino, Università degli Studi di Roma "La Sapienza".
- National scientific research project **FIRB – MAIS – 2001** "Sistemi informativi adattativi multicanale" (Adaptive multi-channel computing systems). National Scientific Coordinator: prof. B. Pernici (Politecnico di Milano). Partners: Politecnico di Milano, Università degli Studi di Roma "La Sapienza", Università degli Studi Roma Tre, Università degli Studi di Lecce, STMicroelectronics, Università degli Studi di Milano-Bicocca, CEFRIEL-Milano, Engineering Ingegneria Informatica – Roma.
- Two-year scientific national research project: **CNR Italian Research Council - 1997-98** Project: "Metodologie e Strumenti per la Progettazione Automatica di Circuiti e Sistemi Digitali a Basso Consumo di Potenza". (Methodologies and Tools for the Automatic Design of Low-Power Digital Circuits and Systems). National Scientific Coordinator: Prof. M. Mezzalama, Politecnico di Torino. Project Partners: Politecnico di Torino, Politecnico di Milano, Università degli Studi di Brescia, Università degli Studi di Ferrara

2.9. PARTICIPATION TO INDUSTRIAL FUNDED RESEARCH PROJECTS

- **Participation** to the two-year research project: "Power estimation methodologies for VLIW architectures" (2000-2002) between DEI - Politecnico di Milano and the Advanced System Technology Division of **STMicroelectronics,** Agrate Brianza. Principal Investigator: prof. M. Sami. The activity carried out in this project has been the subject of **one patent granted** by the USA Dept. of Commerce, Patent and trademark Office [P4-US].

2.10. EVALUATION OF RESEARCH PROJECTS FOR THE EUROPEAN COMMISSION:

1. **Independent Expert Reviewer,** ARTEMIS JU – Project 295440 PaPP (Portable and Predictable Performance on heterogeneous embedded many-cores), 2013-2015.
2. **Independent Expert Reviewer,** FP7 – STREP Project 288570 ParaPhrase (Parallel Patterns for Adaptive Heterogeneous Multicore Systems), 2012-2014.
3. **Independent Expert Reviewer,** FP7 – STREP Project 248976 REFLECT (Rendering FPGAs to Multi-Core Embedded Computing), 2010-2012.
4. **Independent Expert Reviewer** to evaluate research proposals submitted to the "Future and Emerging Technologies" programme (EC FET-Open) on FP7-ICT-2009, 2010-2013.
5. **Independent Expert Reviewer** to participate in the on-site Evaluation Panel to evaluate research proposals submitted to the "Future and Emerging Technologies" programme (EC FET-Open) on FP7-ICT-2009 Batch 13, June 2012.
6. **Independent Expert Reviwer,** Network-of-Excellence Project FP6 - IST-4408 HiPEAC (High-Performance Embedded Architectures and Compilers) coordinated by prof. Mateo Valero, Universidad Politecnica de Catalunya, Barcelona. 2005-2008.

7. **Independent Expert Reviewer,** to participate to the on-site Evaluation Panel for the European IV Call IST (Information Society Technology) - FP6 (6th Framework Programme) on Nanoelectronics, April 2005.

2.11. EVALUATION OF RESEARCH PROJECTS FOR SCIENCE FOUNDATIONS

1. **Steering Group Member,** UK Engineering and Physical Sciences Research Council, 2017.
2. **Expert Reviewer,** Swiss National Science Foundation, Switzerland, 2016.
3. **Expert Reviewer,** Programme Blanc International Edition 2010, ANR (Agence Nationale de la Recherche), France, 2010.
4. **Chair of the Review Panel** for Computer Science, Academy of Finland, Research Council for Natural Sciences and Engineering, 2009.
5. **Member of the Review Panel** for Computer Science, Academy of Finland, Research Council for Natural Sciences and Engineering, 2008.
6. **Primary Evaluator**, INRIA (French National Institute for Computer Science - France), 2007.

3. SCIENTIFIC SERVICES

I am an active member of the research community, and so far I have organized several international conferences and workshops as Program Chair or General Chair and I regularly serve in several technical program committees.

3.1. ORGANIZING COMMITTEE MEMBER

1. **Co-Organizer,** ANDARE'17 Workshop on Autotuning and AutotuniNg and aDaptivity AppRoaches for Energy efficient HPC Systems, co-located with the 26th Edition of the Int. Conference on Parallel Architectures and Compilation Techniques (PACT) held in Portland, USA from September 9 to 13, 2017.
2. **Track Chair,** Architectural and Microarchitectural Design, DATE 2017, IEEE/ACM Design and Test in Europe Conference, Lausanne (Switzerland), March 27-31, 2017.
3. **Program Co-Chair,** PARMA-DITAM Workshop 2017, co-located with HiPEAC 2017 Conference, Stockholm (Sweden), Jan. 25, 2017
4. **Track Chair,** Hardware for Embedded Systems, ICCAD2016, The IEEE/ACM International Conference on Computer-Aided Design 2016, Austin, Texas, USA, November 7-10, 2016
5. **Co-Organizer,** First Workshop on Resource Awareness and Application Autotuning in Adaptive and heterogeneous Computing (Res4Ant), co-located with DATE 2016, Dresden (Germany), March 18, 2016.
6. **Track Co-Chair,** Architectural and Microarchitectural Design, DATE 2016, IEEE/ACM Design and Test in Europe Conference, Dresden (Germany), March 14-18, 2016.
7. **General Co-Chair,** PARMA-DITAM Workshop 2016, co-located with HiPEAC 2016 Conference, Prague (Czech Republic), Jan. 18-20, 2016.
8. **Track Chair,** Embedded System Hardware, ICCAD2015, The IEEE/ACM International Conference on Computer-Aided Design 2015, Austin, Texas, USA, November 2-6, 2015.
9. **Local Organizer**, HiPEAC Computing System Week, held at Politecnico di Milano (Italy), September 21-23, 2015.
10. **Program Chair,** FPL 2015, 25th International Conference on Field Programmable Logic and Applications, London (UK), September, 2015.
11. Program Co-Chair, **ViPES'2015**, 3rd Workshop on Virtual Prototyping of Parallel and Embedded Systems, co-located with SAMOS Conference 2015, July 19th, 2015, Samos.
12. **Subcommittee Chair,** Embedded System Design, DAC 2015, 52nd ACM/IEEE Design Automation Conference, San Francisco CA, June 7-11, 2015.
13. **Track Co-Chair,** Architectural and Micro-architectural Design, DATE 2015, IEEE/ACM Design and Test in Europe Conference, Grenoble (France), March 9-13, 2015.
14. **General Co-Chair,** PARMA-DITAM Workshop 2015, co-located with HiPEAC 2015 Conference, Amsterdam (NL), January 19-21, 2015.
15. **Track Co-Chair,** Design Methods and Tools, FPL 2014, 24th International Conference on Field Programmable Logic and Applications, Munich (Germany), Sept., 2014.
16. **General Chair,** PARMA-DITAM Workshop 2014, co-located with HiPEAC Conference 2014, Wien (A), Jan. 20, 2014.
17. **Track Co-Chair,** SoC Design and Interconnect, VLSI-SOC 2013, 21st IFIP/IEEE International Conference on Very Large Scale Integration, Istanbul (Turkey), October, 2013.
18. **Workshops Co-Chair,** FPL 2013, 23rd International Conference on Field Programmable Logic and Applications, Porto, Sept. 2-4, 2013.
19. **General Co-Chair,** DEPCP 2013, 5th DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Grenoble, March 22nd, 2013.
20. **General Co-Chair,** Fall School on Programming Paradigms for Multi-core Embedded Systems, Freudenstadt – Lauterbad, Germany, October 2-5, 2012.
21. **Program Co-Chair,** ASAP 2012, 23rd IEEE International Conference on Application-specific Systems, Architectures and Processors, Delft (NL), 9-11 July 2012.

22. **Subcommitte Co-Chair,** Embedded Systems Design Methodologies, DAC 2012, ACM/IEEE Design Automation Conference, San Francisco CA, 3-7 June 2012.
23. **General Co-Chair,** DEPCP 2012, 4th DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Dresden, March 16th, 2012.
24. **Co-Organizer,** RAPIDO Workshop 2012 on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2012, Paris.
25. **General Co-Chair,** DEPCP 2011, 3rd DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Grenoble, March 18th, 2011.
26. **Program Co-Chair,** ARCS 2011, Architecture of Computing Systems Conference, Como (Italy), 22-25 Feb. 2011.
27. **Co-Organizer,** RAPIDO Workshop 2011, on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2011, Crete.
28. **Program Co-Chair,** SASP 2010, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference), Anaheim, CA, June 13-18, 2010.
29. **Co-Organizer** and **Architectures Session Chair,** DEPCP 2010, Second DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Dresden, March 12th, 2010.
30. **General Co-Chair,** PARMA Workshop 2010 on Parallel Programming and Run-time Management Techniques for Many-core Architectures, co-located with ARCS 2010 **-** Architecture of Computing Systems Conference, Hannover (D), February 2010.
31. **Co-Organizer,** RAPIDO Workshop 2010 on Rapid Simulation and Performance Evaluation: Methods and Tools, co-located with HiPEAC Conference, January 2010, Pisa.
32. **General Co-Chair,** SASP 2009, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) San Francisco, CA, July 27-28, 2009.
33. **Program Co-Chair,** SAMOS IX Workshop on Systems, Architectures, Modeling and Simulation, Samos, Greece, July, 2009.
34. **Co-Organizer** and **Architectures Session Chair,** DEPCP 2009, First DATE Friday Workshop on Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, Nice, April 24th, 2009.
35. **General Co-Chair,** MICRO 2008, 41st Annual IEEE/ACM International Symposium on Microarchitecture, Como (Italy), 8-12 November 2008.
36. **Publicity Chair,** SASP 2008, IEEE Symposium on Application Specific Processors (Co-located with ACM/IEEE Design Automation Conference) Anaheim, CA, June 8-9, 2008.
37. **Publicity Chair,** WASP2007, Fifth Workshop on Application Specific Processors, 2007.

3.2. PROGRAM COMMITTEE MEMBER

1. **CGO2018,** 2018 IEEE/ACM International Symposium on Code Generation and Optimization.
2. **PACT,** International Conference on Parallel Arhitectures and Compilation Techniques, 2017-2018.
3. **ARC,** International Symposium on Applied Reconfigurable Computing, 2017-2018.
4. **IPDPS,** IEEE International Parallel and Distributed Processing Symposium, 2015-2018.
5. **DAC,** ACM/IEEE Design Automation Conference, 2011-2013, 2015.
6. **DATE,** IEEE/ACM Design and Test in Europe Conference, 2005-2017.
7. **FPL,** International Conference on Field Programmable Logic and Applications, 2013-2016, 2018.
8. **ICCAD,** IEEE/ACM International Conference on Computer-Aided Design, 2014-2016.
9. **NOCS,** ACM/IEEE International Symposium on Networks-on-Chip, 2009-2018.
10. **DSD,** Euromicro Conference on Digital System Design, 2012- 2017.
11. **ASAP,** IEEE International Conference on Application-specific Systems, Architectures and Processors**,** 2012-2018.
12. **ARCS,** Architecture of Computing Systems Conference, 2010-2014, 2017.

13. **IC-SAMOS,** International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, 2006-2018.
14. **HPCC,** IEEE International Conference on High Performance Computing and Communications, 2014.
15. **ICPP,** IEEE International Conference on Parallel Processing, 2011, 2013.
16. **EUC 2013,** IEEE/IFIP Int. Conf. on Embedded and Ubiquitous Computing, 2013.
17. **MES 2013,** International Workshop on Many-core Embedded Systems.
18. **VLSI-SOC,** IFIP/IEEE International Conference on Very Large Scale Integration, 2008-2011, 2013.
19. **HPCA-18,** 18th International Symposium on High Performance Computer Architecture, 2012.
20. **IA^3,** Workshop on irregular Applications: Architectures and Algorithms, 2011-2012
21. **CF,** ACM International Conference on Computing Frontiers, 2009, 2012, 2016, 2017.
22. **WRC,** Workshop on Reconfigurable Computing, co-located with HiPEAC Conference, 2010-2012.
23. **PDP,** Euromicro Int. Conference on Parallel, Distributed and Network-Based Computing, 2012
24. **SASP,** IEEE Symposium on Application Specific Processors, 2008-2011.
25. **MICRO-43,** 43rd Annual IEEE/ACM International Symposium on Microarchitecture, 2010.
26. **HiPEAC,** Int. Conference on High-Performance Embedded Architectures and Compilers, 2010.
27. **ICS,** the 20th ACM International Conference on Supercomputing, 2006.
28. **WASP,** Workshop on Application Specific Processors, 2004-2007.

3.3. ASSOCIATE/GUEST EDITOR AND JOURNAL REVIEWER

- **Associate Editor,** ACM Transactions on Architecture and Code optimization (TACO) (2015-present).
- **Associate Editor,** MICPRO Journal, Embedded Hardware Design (Microprocessor and Microsystems), Elsevier (2013- 2015)
- **Guest Co-Editor,** Special Issue with selected papers from FPL 2015, 25th International Conference on Field Programmable Logic and Applications, to be published in 2016 on ACM Transactions on Reconfigurable Technology and Systems (TRETS).
- **Guest Co-Editor,** Special Issue with selected papers from ViPES2015, to be published in 2016 on ACM Transactions on Embedded Computing Systems (TECS).
- **Guest Co-Editor,** Special Issue with selected papers from DSD2012 on Reliability and Dependability in MPSoC Technologies, Journal on Microprocessors and Microsystems: Embedded Hardware Design (MICPRO), Elsevier, Vol. 37, Number 8-A, 2013 (09/2012 – 12/2012).
- **Selection Committee Member,** IEEE MICRO Special Issue on "Top Picks 2010 from Computer Architecture Conferences", January/February 2011.
- **Guest Co-Editor,** Special Issue with selected papers from International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS2009) on Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC), Volume 5, Issue 3, Springer. (09/2009 – 03/2010)
- **Subject Area Editor,** Journal of Systems Architecture – The EUROMICRO Journal, Elsevier Ed. (06/2003 - 10/2005).

From 1993 to present, I am servicing as **reviewers** for several prestigious international journals such as: IEEE Transactions on Computers; IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems; IEEE Transactions on Very Large Scale Integration Systems; IEEE Design and Test; IEEE Micro; ACM Transactions on Design Automation of Electronic Systems; ACM Transactions on Embedded Computing Systems; Springer Journal on VLSI Signal Processing Systems; Springer Journal on Design Automation for Embedded Systems; Elsevier Journal on Microprocessors and Microsystems: Embedded Hardware Design (MICPRO); IET Computers and Digital Techniques;

3.4. INVITED TALKS, SEMINARS AND PANELS

1. September 18, 2017, "Application autotuning for energy efficient heterogeneous HPC systems", **Invited Talk** at the ScalPerf'2017 Workshop on "Scalable Approaches to High Performance and High Productivity Computing", Bertinoro, Italy from September 17 to 22, 2017.

2. August 28, 2017, "Application autotuning for energy efficient heterogeneous HPC systems", **Keynote Speaker** at HeteroPar'2017, the15th International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms, co-located with the 23rd Edition of EuroPar'2017, the Int. European Conference on Parallel and Distributed Computing held in Santiago de Compostela, Spain from August 28 to September 1, 2017.
3. June 9, 2016, "Design Space and Application Autotuning for Runtime Adaptivity in Multicore Architectures", **Seminar** at Brain Inspired Computing Group, IBM Research, Austin, Host: Dr. Jun Sawada, IBM Research, Austin.
4. June 3, 2016, "Design Space and Application Autotuning for Runtime Adaptivity in Multicore Architectures", **Seminar** at the University of Texas at Austin, Electrical and Computer Engineering, Computer Architecture Seminar Series, Austin, Host: prof. Andreas Gerstlauer, prof. Yale Patt, University of Texas at Austin, Link
5. May 17, 2016, **Panel Moderator** on: "Power Efficiency: Where are you?" Panelists: Adolfy Hoisie, Marek Michalewicz, Roberto Giorgi, Tobias Gemmeke, held at ACM International Conference on Computing Frontiers 2016, Como, Italy.
6. March 18, 2016, **Panel Moderator** on: "Moore's law is still alive! So why resource awareness?", Panelists: Cathal McCabe, Axel Auweter, João M. P. Cardoso, Axel Jantsch, X. Sharon Hu, Andreas Rohatschek and Michael Hübner; held at First Workshop on Resource Awareness and Application Autotuning in Adaptive and Heterogeneous Computing, co-located with DATE2016 Conference on Design , Automation and Test in Europe, Dresden, Germany.
7. October 21st, 2015, "Design Space Exploration and Application Autotuning for Runtime Adaptivity in Multicore Architectures" **Keynote Speaker** at the 13th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC2015) / 18th IEEE International Conference on Computational Science and Engineering (CSE2015), Porto (Portugal).
8. October 23rd, 2015, "ANTAREX: AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems", **Invited Talk** at the Special Session on FET-HPC and Exascale Recently EU-funded projects, 13th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC2015) / 18th IEEE International Conference on Computational Science and Engineering (CSE2015), Porto (Portugal).
9. September 29-30, 2015, "ANTAREX: AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems", **Invited Talk** at the ETP4HPC (European Technology Platform for High Performance Computing) - EXDCI (European eXtreme Data and Computing Initiative) Workshop, Rome (Italy).
10. September 21st, 2015, "ANTAREX: AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems", **Invited Talk** at the Thematic Section on Challenges and opportunities in next-generation HPC Systems for Real-Time Applications, HiPEAC Computing System Week, Milan (Italy), Host: Prof. José Flich, Univ. Politècnica de València. SLIDES
11. October 8th, 2014, "Managing Adaptability in Heterogeneous Architectures through Performance Monitoring and Prediction", **Invited Talk** at the Thematic Section on Heterogeneous System Tools for Simulation, Debugging, Performance Modeling and Resource Management, HiPEAC Computing System Week, Athens, Host: Prof. Georgios Goumas, National Technical University of Athens.
12. May 15th, 2014, "Managing Adaptability in Dynamically Reconfigurable Architectures through Performance Monitoring and Prediction", **Invited Talk** at the Thematic Section on Reconfigurable Computing, HiPEAC Computing System Week, Barcelona, Host: Prof. Georgi Gaydadjiev, Chalmers University of Technology.
13. September 4th, 2013, **Panel Moderator** on: "EU Horizon 2020 on Reconfigurable Computing" Invited Speakers: Dr. Panos Tsarchopoulos, Future and Emerging Technologies, EU Project Officer; Dr. Georgi Kuzmanov, ARTEMIS Joint Undertaking, EU Programme Officer; held at FPL2013, 23rd International Conference on Field Programmable Logic and Applications, Porto.
14. June 8th, 2012, "Automatic Design Space Exploration for Multi-core Architectures", **Seminar** at Intel Labs, Santa Clara (CA, USA), Host: Dr. Akhilesh Kumar, Intel.
15. April 25th, 2012. "Design-time support for run-time management of embedded multiprocessor architectures", **Invited Talk** at the Thematic Section on Design and runtime management of

reconfigurable systems, HiPEAC Computing System Week, Goteborg, Host: Prof. Georgi Gaydadjiev, Chalmers University of Technology.

16. February 7th, 2012, "Design Space Exploration and Run-time Resource Management for Multi-core Architectures", **Seminar** at the University of Texas at Austin, Electrical and Computer Engineering, Computer Architecture Seminar Series, Austin, Host: Prof. Yale Patt, University of Texas at Austin.
17. September 7th, 2011, "2PARMA Project" **Invited Talk** at FPL2011 European Project Workshop, Chania, Crete. Organizer. Prof. Joao Cardoso, Univ. of Porto.
18. April 7th, 2011, "2PARMA Project: PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures", **Invited Talk,** HIPEAC Cluster Meeting on Multi-core Architectures, 2011 Chamonix (F), Host: Prof. Per Stenström, Chalmers University of Technology.
19. November 24th, 2010, "Automatic Design Space Exploration for Chip Multi-processors", **Invited Talk** at the Workshop on "Challenges in Embedded System Design": Involvement of SMEs in Designing Complex Systems (CMM 2010), University of Lugano (CH), Workshop Organizers: Prof. G. De Micheli (EPFL) and Prof. M. Sami (USI-Politecnico di Milano).
20. July 6th, 2010, "MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures", **Invited Talk** at the Research Projects Workshop at ISVLSI 2010: IEEE Computer Society Annual Symposium on VLSI, July 5-7, 2010, Lixouri Kefalonia, Greece.
21. June 18th, 2010, "Automatic Design Space Exploration for Chip-Multi Processors". **Seminar** at University of California Riverside, Department of Computer Science & Engineering, Riverside (CA, USA), Host: Prof. Walid Najjar, University of California Riverside.
22. June 17th, 2010, "Automatic Design Space Exploration for Chip-Multi Processors". **Seminar** at University of California Irvine, Department of Computer Science & Engineering, Irvine (CA, USA), Host: Prof. Alexander V. Veidenbaum, University of California Irvine.
23. March 23rd, 2010, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "A Design Space Exploration Framework for Run-Time Resource Management on Multi-Core Architectures". Host: Prof. Koen Bertels, Delft Technical University.
24. December 17th, 2009, **Seminar** at NEC Laboratories America, Inc., Princeton Campus, Princeton (NJ - USA), Title: "Automatic Design Space Exploration for Chip-Multi Processors". Host: Dr. Marcello Lajolo, NEC Labs America.
25. December 16th, 2009, **Seminar** at Princeton University, Department of Electrical Engineering, Computer Engineering Seminar, Title: "Automatic Design Space Exploration for Chip-Multi Processors", Host: Prof. Ruby Lee, Princeton University.
26. July 29th, 2009, **Seminar** at HP Labs, Palo Alto, Title: "MULTICUBE Explorer: Leveraging DoE/RSM-based Techniques to Automate Design Space Exploration for CMPs", Host: Dr. Matteo Monchiero, HP Labs, Palo Alto.
27. May 14th, 2009, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "MULTICUBE Explorer: Leveraging DoE/RSM-based Techniques to Automate Design Space Exploration for CMPs" Host: Prof. Koen Bertels, Delft Technical University.
28. April 25th, 2006, **Seminar** at Delft Technical University, Computer Engineering Colloquium Series. Title: "Exploration and Optimization of Multiprocessor Embedded Architectures based on Networks-on-Chip", Host: Prof. Stamatis Vassiliadis, Delft Technical University.
29. September 22nd, 2005, New York, USA, **Panelist at WASP 2005** Workshop on Application Specific Processors (co-located with International Conference on Hardware/Software Codesign and System Synthesis), Panel title: "Application Specific Customizations: Processor or System Level?" Moderator: Prof. Daniel Gajski, UC Irvine.

3.5. MEMBER OF PROFESSIONAL ORGANIZATIONS

- Since 2017, **IEEE Computer Society Fellow** "for contributions to energy-efficient computer architectures."
- Since 2009, **IEEE Senior Member** (Member since 1993).
- Since 2013, **ACM** (Association of Computing Machinery) **Member**.
- Since 2008, **Member** of the **HiPEAC** Network of Excellence.

4. ACADEMIC SERVICES

4.1. TEACHING ACTIVITIES AT UNIVERSITIES

In the past years, I have balanced my efforts in teaching both at the Undergraduate level and at the Master of Science level at Politecnico di Milano and previously at the Università degli Studi di Milano. At the Undergraduate level, I taught several courses in the Computer Engineering track: **Computer Architectures, Operating Systems, Logic Design** and **Computer Science Fundamentals.** At the M. Sc. level, I taught courses mainly related to my research areas: **Advanced Computer Architectures** and **Hardware/Software Co-design Methodologies.**

I have an extensive **English-speaking teaching experience** in a multicultural environment thanks to my courses at the M.Sc. program in Computer Engineering at the Como Campus of Politecnico di Milano (2003-present), at the Leonardo Campus of Politecnico di Milano (2014-present) and at the Università della Svizzera Italiana (2012). From 2002 to present, I was **advisor of more than 60 M.Sc. students** in Computer Engineering at Politecnico di Milano. Since 20002, I was member of several Thesis Committees at the Undergraduate and M. Sc. level in Computer Engineering at Politecnico di Milano.

At the Undergraduate level, I am currently teaching the second part of the course on: **"Computer Architecture and Operating Systems",** which is a mandatory course for the B.Sc. students in Computer Engineering at Politecnico di Milano: The course introduces the basic concepts of computer architectures and operating systems. The first part of the course is covering logic design, computer architecture (MIPS processor) and programming in assembly language. The second part of the course is covering the structure of the Operating System in terms of management of processes, virtual memory, file system and I/O devices. The goal of the course is to provide the students a view of the computer architecture from a hardware/software comprehensive perspective at several levels (programming, operating system, architecture, micro-architecture and logic design).

At the Master of Science level, I am currently teaching the course: **"Advanced Computer Architectures"**, which is a mandatory course for the M.Sc. students in Computer Engineering at Politecnico di Milano. **The course is completely offered in English.** The goal of the course is to expose the students the main challenges related to the most recent and advanced computer architectures to reach high performance and energy efficiency. The emphasis is on metrics for performance evaluation and techniques for the performance optimization of the processor and memory architecture. The first part of the course is related to Instruction Level Parallelism including pipelining, superscalar processors, VLIW (Very Long Instruction Word) processors, branch prediction techniques and speculative execution. The second part of the course is related to thread-level parallelism and multi-processors including manycores, System-on-Chip and Network-on-Chip architectures. My effort is spent every year to update the course materials to reflect the state-of-the-art concepts on advanced processor architectures. At the end of the course, the students are aware on the most recent processor architectures designed for high-performance and embedded computing.

Apart from course developments, **I enjoy teaching and I have a strong interest in developing new pedagogical approaches to teach topics related to Computer Architectures.**

My efforts are devoted to directly transfer to the students my research knowledge and experience and results not only through continuously updating the concepts exposed in the courses to reflect state-of-the-art concepts, but also during the advising of the students for the development of course projects and M.Sc. thesis. In this context, some of the tools developed in our research (such as MULTICUBE Explorer or PIRATE Simulator) have been used in the courses. This process is to make sure the students are updated on state-of-the-art research on computer architectures and are practicing the related tools. It is also important to have a constructive and continuous interaction with the students and to allow them to contribute to the improvements and quality assessment in teaching. I believe top quality teaching and good international visibility are key issues to guarantee adequate levels of in-flow of high quality students. A way to enhance the industrial exposure of our M.Sc. students is by offering internships during which they can work on industrial projects. In the past years, I have followed several students doing an internship (in the context of their Master thesis) with STMicroelectronics.

More recently, I am preparing to apply some pedagogical concepts from the ***"flipped classroom approach"*** to my courses. Based on this approach, the students are learning theoretical concepts outside of the classroom setting and then the students directly apply these concepts in class with the assistance of the tutor and the other students. This approach facilitates a more active and responsible learning approach from the side of the

students, that can obtain an immediate feedback on their level of knowledge and comprehension during the class activities. The overall idea is to increase the students' engagement, to encourage their critical thinking and to improve their natural attitudes. Up to now, this approach has already been used in several fields of studies, including Biology, Mathematics, Statistics, Physics, Engineering and Computer Science. During the next semesters, I am planning to revise my teaching approach to adopt the flipped classroom approach on some advanced topics to invite students to study a specific part of the course material before the class. The next lecture time will then be dedicated to revise the topic in class and to engage the students to present specific problems in order to exercise their higher order thinking skills and to promote their critical thinking by discussing advantages and drawbacks of the proposed solutions. The objective is to have a higher interactive class where the students are encouraged to express their opinions, to participate to class discussions and to propose innovative solutions to problems. My final goals are to guide students in their learning experiences, to increase their ability to reasoning and to understanding benefits and limitations of the studied approaches.

Hereafter is the list of courses held as **Professor** at the **School of Industrial and Information Engineering, Politecnico di Milano** during the **past five Academic Years:**

Course Title	Credits	Sem.	Computer Engineering Programme	Campus	Language	No. of Enrolled Students	Students Evaluat.
2017/2018							
Advanced Computer Architectures	5	2nd	M.Sc.	Milano Leonardo	English	190	N.A.
Advanced Computer Architectures	5	2nd	M.Sc.	Como	English	33	N.A.
Operating Systems	5	1st	B.Sc.	Como	Italian	76	N.A.
2016/2017							
Advanced Computer Architectures	5	2nd	M.Sc.	Milano Leonardo	English	186	High
Advanced Computer Architectures	5	2nd	M.Sc.	Como	English	50	High
Operating Systems	5	1st	B.Sc.	Como	Italian	85	Medium
2015/2016							
Advanced Computer Architectures	5	2nd	M.Sc.	Milano Leonardo	English	144	High
Advanced Computer Architectures	5	2nd	M.Sc.	Como	English	74	High
Operating Systems	5	1st	B.Sc.	Como	Italian	70	High
2014/2015							
Advanced Computer Architectures	5	2nd	M.Sc.	Milano Leonardo	English	128	Medium
Advanced Computer Architectures	5	2nd	M.Sc.	Como	English	73	High
2013/2014							
Advanced Computer Architectures	5	2nd	M.Sc.	Milano Leonardo	Italian	181	High
Advanced Computer Architectures	5	2nd	M.Sc.	Como	English	74	Medium
Operating Systems	5	1st	B.Sc.	Como	Italian	60	Medium

Before these recent courses, I taught the following courses at Politecnico di Milano:

- "Computer Architectures and Operating Systems" (10 credits), B. Sc. Level, Como Campus from 2009/10, to 2011/12.
- "Architectures for Multimedia Systems" (5 credits), M.Sc. Level (English), Como Campus, from 2003/2004 to 2009/10.
- "Hardware/software Co-design Methodologies" (5 credits), Ms.C. Level, from 2004-05 to 2008/09.
- "Computer Science Fundamentals" (10 Credits), M. Sc. Level, Como Campus, from 2002/03 to 2007/08.
- "Computer Architectures" (10 Credits), M.Sc., Electronics and Telecomm. Eng., Milano Leonardo Campus, from 2001/02 to 2002/03.

Previously, I also taught the following courses:

- "Advanced Computer Architectures" (3 credits), M.Sc. Embedded Systems (English), Università della Svizzera Italiana, Fall 2012.
- "Computer and Network Architectures" (12 Credits), B.Sc. Level, Computer Science, Università degli Studi di Milano from 2000/01 to 2006/07.
- "Laboratory of Architectures and Operating Systems" (6 Credits), B.Sc. Level, Computer Science, Università degli Studi di Milano from 1999/00 to 2001/2002.

Finally, I am co-author of the **academic textbook** (in Italian): "Progettazione digitale" (Logic Design) edited by McGraw-Hill, First Edition 2002 -- Second Edition 2007. The textbook is currently used in Italy at the B.Sc. level in basic courses of Logic Design in Computer Engineering and Computer Sciences.

4.2. ACADEMIC RESPONSIBILITIES

Since 2002, I am an active contributor to the organisation of the teaching activities and tracks in Computer Engineering at Politecnico di Milano, Como Campus, where I have had several responsibilities and I was participating to the following committees as:

- ***Chair,*** Committee on Undergraduate Study Plans (Commissione Piani degli Studi - Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2002-Present.
- ***Chair,*** Committee on Undergraduate Transfers (Commissione Passaggi e Trasferimenti - Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.
- ***Member,*** Committee on Graduate Admissions (Commissione Ammissioni alla Laurea Magistrale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.
- ***Member,*** Committee on Undergaduate Studies (Commissione Didattica – Laurea Triennale) in Computer Engineering, Politecnico di Milano, Como Campus, 2003-Present.
- ***Member,*** Committee on Graduate Admissions (Commissione Ammissioni alla Laurea Magistrale) in Computer Engineering, Politecnico di Milano, Leonardo Campus, 2015-Present.

I have also been part of the following temporary committees:

- ***President,*** Committee for the comparative evaluation for two position of Temporary Researcher Type-A in Computer Engineering, RTDA-DEIB39, Politecnico di Milano, 2017.
- ***Member,*** Committee for the comparative evaluation for the position of Temporary Researcher Type A in Computer Engineering, Politecnico di Milano, 2010.
- ***Member,*** Committee for the comparative evaluation of the candidates for one position as Assistant Professor in Computer Engineering, University of Catania, 2007-2008.

4.3. RESEARCH ADVISING

4.3.1. Undergraduate and Master Students Supervision

- Advisor of more than **60** Master students in Computer Engineering, Electrical Engineering, and Communication Engineering at Politecnico di Milano, 2002-Present.
- Advisor of some undergraduate and Master students in Computer Science at Università degli Studi di Milano, 2000-2002.
- Co-advisor of some Master students in Electrical Engineering at Università degli Studi di Brescia, 1996-1999.
- Advisor / co-advisor of some Master students in Information Technology at CEFRIEL Research and Training Center in Milano, EDA (Electronic Design Automation) Group, 1993-1999.

4.3.2. Doctoral and Post-Doctoral Students Supervision

1. **Vittorio Zaccaria,** Ph. D. 2002, Politecnico di Milano. Ph.D. Thesis: "Power exploration methodologies for VLIW-based systems", Advisor: prof. M. Sami. Co-advisors: prof. D. Sciuto, Dr. C. Silvano. Ph.D. Grant from STMicroelectronics. **Recipient of the Dimitris N. Chorofaras – Fondazione Carlo Pesenti Ph.D. Thesis Award 2002.** First employment: R&D Engineer at STMicroelectronics. Currently Assistant Professor at Politecnico di Milano, DEIB.
2. **Gianluca Palermo,** Ph.D. 2006, Politecnico di Milano. Ph.D. Thesis: "Design Methodologies for Embedded Architectures based on Network on-Chip", Advisor: prof. C. Silvano. **Recipient of the Dimitris N. Chorofaras – Fondazione Carlo Pesenti Ph.D. Thesis Award 2006.** First employment: Post-Doctoral Fellow (2006-2010) in my group at Politecnico di Milano. Currently Associate Professor at Politecnico di Milano, DEIB.
3. **Giovanni Beltrame,** Ph.D. 2006, Politecnico di Milano. Ph.D. Thesis: "Modeling, Simulating, Analysis and Optimization of Multi-Processor System-on-Chip Platforms", Advisor: prof. D. Sciuto. Co-advisor: prof. C. Silvano. First employment: Microelectronics Engineer at European Space Agency (NL). Currently Associate Professor at École Polytechnique de Montréal.
4. **Matteo Monchiero,** Ph.D. 2007, Politecnico di Milano. Ph.D. Thesis: "Power/performance analysis and optimization of multicore architectures", Advisor: prof. C. Silvano. Visiting Scholar at Universidad Politecnica de Catalunia UPC. First employment: Post-Doctoral Research Associate at HP Labs in Palo Alto, Exascale Computing Lab. Then Senior Research Scientist, Intel Labs at Santa Clara (CA, US). Currently Principal Engineer at Trifacta, San Francisco.
5. **Oreste Villa,** Ph.D. 2008, Politecnico di Milano. Ph.D. Thesis: "Designing and Programming Multi-core Architectures", Advisor: prof. C. Silvano. Ph.D. Grant from STMicroelectronics. Visiting Scholar at UCLA. First employment: Research Scientist at Pacific Northwest National Laboratory, Richland, WA (USA). Currently Senior Research Scientist, at NVIDIA Architecture Research (US).
6. **Sotirios Xydis,** Ph.D. 2010, National Technical University of Athens. Post-Doctoral Fellow in my group at Politecnico di Milano (From Nov. 2011 to July 2013). His research focused on design space exploration, high-level synthesis and programmable architectures. Currently Post-Doctoral Researcher at National Technical University of Athens.
7. **Giovanni Mariani,** Ph. D. 2011, Università della Svizzera Italiana (USI). Ph.D. Thesis: "A Design Space Exploration Methodology Supporting Run-time Resource Management for Multi-Core Architectures", Advisor: prof. M. Sami, Co-advisor: prof. C. Silvano. Visiting Scholar at TU Delft (NL). Post-Doctoral Fellow (2011-2013) in my group at Politecnico di Milano. Then Post-Doctoral Researcher at ASTRON & IBM Center for Exascale Technology (NL). Currently Post-Doctoral Researcher at IBM Zurich (CH).
8. **Leandro Fiorin,** Ph. D. 2012, Università della Svizzera Italiana (USI). Ph.D. Thesis: "High level services for Networks-on-Chip", Advisor: prof. M. Sami, Co-advisor: prof. C. Silvano. Internship: STMicroelectronics, Grenoble. First employment: Post-Doctoral Researcher at ALaRI –USI (CH). Currently Post-Doctoral Researcher at ASTRON & IBM Center for Exascale Technology (NL).
9. **Edoardo Paone,** Ph. D. 2014, Politecnico di Milano, DEIB, XXVII cycle. Ph.D. Thesis: "Design Space Exploration of OpenCL Applications on Heterogeneous Parallel Platform". Advisor: prof. C. Silvano. First employment: Embedded Software Engineer at Ericsson, Stockholm (Sweden).
10. **Ioannis Stamelakos,** Ph. D. 2016, Politecnico di Milano, DEIB, XXVIII cycle. Ph.D. Thesis: "Near-Threshold Computing with Performance Guarantees for Manycore Architectures". Advisor: prof. C. Silvano. Co-advisor: Dr. S. Xydis, NTUA. Visiting Scholar at University of California at Irvine (CA). First employment: Software Engineer at Oraclize, UK.
11. **Amir Hossein Ashouri,** Ph. D. 2016, Politecnico di Milano, DEIB, XXVIII cycle. Ph.D. Thesis: "Compiler Autotuning using Machine Learning Techniques". Advisor: prof. C. Silvano, Co-Advisors: prof. G. Palermo, Prof. John Cavazos. **IEEE Computer Society (Italy Section) Award for the Best PhD Thesis** defended in an Italian University in 2017 in the field of Computer Science and Engineering. Visiting Scholar at University of Delaware (US). First employment: Post-Doctoral Researcher at University of Toronto (CN).
12. **Davide Gadioli,** Ph. D. student at Politecnico di Milano, DEIB, XXIX cycle. Ph.D. Thesis: "Application Auto-Tuning and Run-Time Resource Management for Adaptive OpenCL Applications". Advisor: prof. G. Palermo. Co-advisor: prof. C. Silvano. Ph.D. defense expected in 2018.
13. **Ahmet Erdem,** Ph. D. student at Politecnico di Milano, DEIB, XXXII cycle. Ph.D. Thesis: "Hybrid Multiprocessor Architectures and Tools for Deep Learning and Convolutional Neural Network Applications". Ph.D. Grant from STMicroelectronics. Advisor: prof. C. Silvano. Co-advisor: Dr. G. Desoli, STMicroelectronics. Ph.D. defense expected in 2020.

4.3.3. PhD External Examiner

1. In March 2018, Opponent Member of the Doctoral Examination Committee, National Technical University of Athens (Greece), for the Ph.D. defense of the candidate **Vasileios Tsoutsouras** discussing a thesis titled: "Design Methodologies for Resource Management of Many-core Embedded Systems", Advisors: prof. Dimitrios Soudris.
2. In July 2017, Opponent Member of the Doctoral Examination Committee, Rheinisch-Westfaalischen Technischen Hochschule Aachen (Germany), for the Ph.D. defense of the candidate **Daniel Guenther** discussing a thesis titled: "Hardware and Software Design Methodologies for Portability, Flexibility and Versatility in Multi-Standard MIMO Baseband Processing", Advisors: prof. Gerd Ascheid.
3. In June 2017, Opponent Member of the Doctoral Examination Committee, Norwegian University of Science and Technology (NTNU), Trondheim, Norway for the Ph.D. defense of the candidate **Alexandru Ciprian Iordan** discussing a thesis titled: "Improving the energy-efficiency of task based programming on chip multiprocessors", Advisors: prof. Lasse Natvig.
4. In November 2014, Opponent Member of the Doctoral Examination Committee, Eindhoevn University of Technology (NL), for the Ph.D. defense of the candidate **Dongrui She** discussing a thesis titled: "Energy Efficient Code Genertion for Streaming Applications", Advisors: prof. Henk Corporaal.
5. In April 2013, Opponent Member of the Doctoral Examination Committee, Technical University of Catalonia UPC (Spain) for the Ph.D. defense of the candidate **Nikita Nikitin** discussing a thesis titled: "Automatic Synthesis and Optimization of Chip Multiprocessors", Advisors: prof. Jordi Cortadella.
6. In June 2011, Opponent Member of the Doctoral Examination Committee, Technical University of Catalonia – UPC (Spain) for the Ph.D. defense of the candidate **Friman Sánchez Castaño** discussing a thesis titled: "Exploiting Multiple Levels of Parallelism in Bioinformatics Applications", Advisors: prof. Alex Ramírez and prof. Mateo Valero.
7. In April 2011, Opponent Member of the Doctoral Examination Committee, University of Verona, for the Ph. D. defense of the candidate **Francesco Stefanni** discussing a thesis titled: “A design and verification methodology for networked embedded systems”, Advisor: prof. Franco Fummi.
8. In February 2011, Opponent Member of the Doctoral Examination Committee, Board of the Doctorates, Delft University of Technology (NL) for the Ph.D. defense of the candidate **Kamana Sigdel** discussing a thesis titled: "System-level Design Space Exploration of Reconfigurable Architectures". Advisors: prof. K. Bertels and prof. A. Pimentel.
9. In May 2009, Opponent Member of the Doctoral Examination Committee, Board of the Doctorates, Delft University of Technology (NL) for the Ph.D. defense of the candidate **Carlo Galuzzi** discussing a thesis titled: "Automatically fused instructions". Advisor: prof. K. Bertels.

5. LIST OF PUBLICATIONS

5.1. INTERNATIONAL JOURNALS WITH PEER REVIEW

[J1]. Amir H. Ashouri, William Killian, John Cavazos, Gianluca Palermo, Cristina Silvano, "A Survey on Compiler Autotuning using Machine Learning", **ACM Computing Surveys,** *Accepted for Publication,* March 2018. DOI

[J2]. Amir Hossein Ashouri, Andrea Bignoli, Gianluca Palermo, Cristina Silvano, Sameer Kulkarni, John Cavazos, "MiCOMP: Mitigating the Compiler Phase-Ordering Problem Using Optimization Sub-Sequences and Machine Learning", **ACM Transactions on Architecture and Code Optimization (TACO),** Vol. 14, No. 3, Article 29, September 2017. DOI

[J3]. Philip Heng Wai Leong, Hideharu Amano, Jason Helge Anderson, Koen Bertels, João M. P. Cardoso, Oliver Diessel, Guy Gogniat, Mike Hutton, JunKyu Lee, Wayne Luk, Patrick Lysaght, Marco Platzner, Viktor K. Prasanna, Tero Rissa, Cristina Silvano, Hayden Kwok-Hay So, Yu Wang, "The First 25 Years of the FPL Conference: Significant Papers", **ACM Transactions on Reconfigurable Computing (TRETS),** Vol. 10, No. 1, Article 15, pp. 1-17, June 2017, DOI

[J4]. Amir Hossein Ashouri, Giovanni Mariani, Gianluca Palermo, Eunjung Park, John Cavazos, Cristina Silvano, "COBAYN: Compiler Autotuning Framework Using Bayesian Networks", **ACM Transactions on Architecture and Code Optimization (TACO),** Vol. 13, No. 2, Article 21, June 2016, DOI

[J5]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "DeSpErate++: An Enhanced Design Space Exploration Framework using Predictive Simulation Scheduling", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Vol. 34, No. 2, February 2015. pp. 293-306. DOI

[J6]. Sotirios Xydis, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High Level Synthesis", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Vol. 34, No. 1, January 2015, pp 155-159. DOI

[J7]. Leandro Fiorin, Gianluca Palermo and Cristina Silvano. "A Configurable Monitoring Infrastructure for NoC-Based Architectures", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems.** Vol. 22, No. 11, November 2014, pp. 2436-2440, DOI

[J8]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "Design Space Exploration and Run-time Resource Management for Multi-cores", **ACM Transactions on Embedded Computing Systems (TECS),** Vol. 13, Issue 2, Special Issue on Application Specific Processors, September 2013, pp. 20:1-20:27 DOI

[J9]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "ARTE: An Application-specific Run-Time managEment framework for multi-cores based on queuing models", **Parallel Computing, Elsevier Journal,** Vol. 39, Issue 9, September 2013, pp. 504-519 Available online 20 April 2013, ISSN 0167-8191, DOI

[J10]. Andrea Di Biagio, Giovanni Agosta, Cristina Silvano and Martino Sykora, "Architecture Optimization of Application-Specific Implicit Instructions". **ACM Transactions on Embedded Computing Systems (TECS),** Vol. 11, Issue S2, Article No. 44 (August 2012), pages 44:1 --44:23 (23 pages), DOI

[J11]. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria, "A Variability-Aware Robust Design Space Exploration Methodology for On-Chip Multiprocessors Subject to Application-Specific Constraints". **ACM Transactions on Embedded Computing Systems (TECS),** Vol. 11, Issue 2, Article 29 (July 2012), pages 29:1 --29:28 (28 pages). DOI

[J12]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, "OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Space", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Vol. 31, No. 5, May 2012, pp. 740-753, DOI

[J13]. Chantal Ykman-Couvreur, Prabhat Avasare, Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "Linking run-time resource management of embedded multi-core platforms with automated design-time exploration", **IET Computers and Digital Techniques,** March 2011, Vol. 5, Issue 2, pp. 123-135 DOI

[J14]. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "ReSPIR: A Response Surface-Based Pareto Iterative Refinement for Application-Specific Design Space Exploration", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Vol. 28, No. 12, Dec. 2009, pp. 1816-1829, DOI

[J15]. Leandro Fiorin, Gianluca Palermo, Slobodan Lukovic, Valerio Catalano, Cristina Silvano, "Secure Memory Accesses on Networks-on-Chip", **IEEE Transactions on Computers,** Vol. 57, No. 9, pp. 1216-1229, Sept., 2008, ISSN: 0018-9340, DOI

[J16]. Giovanni Beltrame, Donatella Sciuto, Cristina Silvano, "Multi-Accuracy Power and Performance Transaction-Level Modeling", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Volume: 26, No. 10, October 2007, Pages: 1830 -1842, DOI

[J17]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa, "Exploration of Distributed Shared Memory Architectures for NoC-based Multiprocessors", **Journal of Systems Architecture: The Euromicro Journal** - Elsevier, Volume 53, Number 10, October 2007, pp. 719-732, DOI

[J18]. Cristina Silvano, Giovanni Agosta, Gianluca Palermo, "Efficient Architecture/Compiler Co-Exploration Using Analytical Models", **Design Automation for Embedded Systems,** Springer, Volume 11, Issue 1, March 2007, pp. 1-23, ISSN 0929-5585 (Print) 1572-8080 (Online), DOI: 10.1007/s10617-006-9588-7, DOI

[J19]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa, "Efficient Synchronization for Embedded on-Chip Multiprocessors", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems,** Vol. 14, No. 10, October 2006, pp. 1049-1062, DOI

[J20]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "An Efficient Synchronization Technique for Multiprocessor Systems on-Chip". **ACM SIGARCH Computer Architecture News** (ACM, New York, USA) Volume 34, Issue 1 (March 2006) pp. 33-40. ISSN: 0163-5964, Special Issue on MEDEA-05 - International Workshop on MEmory performance: DEaling with Applications, systems and architecture" DOI

[J21]. Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria, "Multi-Objective Design Space Exploration of Embedded Systems", **Journal of Embedded Computing, IOS Press,** Vol. 1, No. 3, 2005, pp. 305-316, ISSN 1740-4460, url

[J22]. Andrea Bona, Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria and Roberto Zafalon, "Reducing the Complexity of Instruction-Level Power Models for VLIW Processors", **Design Automation for Embedded Systems,** Springer US, March 2005, Vol. 10, No. 1, pp. 49-67, DOI

[J23]. Matteo Monchiero, Gianluca Palermo, Mariagiovanna Sami, Cristina Silvano, Vittorio Zaccaria and Roberto Zafalon, "Low-Power Branch Prediction Techniques for VLIW Architectures: A Compiler-Hints Based Approach", **Integration, The VLSI Journal,** Elsevier, Volume 38, Issue 3, January 2005, pp. 515-524, DOI

[J24]. Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria and Roberto Zafalon, "Low-Power Data Forwarding for VLIW Embedded Architectures", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems,** Vol. 10, No. 5, October 2002, Pages: 614 – 622, DOI

[J25]. Luca Benini, Davide Bruni, Mauro Chinosi, Cristina Silvano, Vittorio Zaccaria, and Roberto Zafalon, "A Framework for Modeling and Estimating the Energy Dissipation of VLIW-based Embedded Systems", **Design Automation for Embedded Systems,** Kluwer Academic Publishers, Boston, October 2002, Volume 7, Issue 3, Pages: 183-203, DOI

[J26]. Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria, "An Instruction-Level Energy Model for Embedded VLIW Architectures", **IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,** Volume: 21, Issue: 9 , Sept. 2002, Pages: 998 -1010, DOI

[J27]. William Fornaciari, Donatella Sciuto, Cristina Silvano, Vittorio Zaccaria, "A Sensitivity-Based Design Space Exploration Methodology for Embedded Systems", **Design Automation for Embedded Systems,** Vol. Special Issue on "Design Methodologies and Tools for Real-Time Embedded Systems", Kluwer Academic Publishers, Boston, Sept. 2002, Volume 7, Issue 1-2, Pages: 7-33, DOI

[J28]. Franco Fummi, Donatella Sciuto, Cristina Silvano, "Automatic Generation of Error Control Codes for Computer Applications", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems,** Vol. 6, No. 3, Sept. 1998, pp. 502-506, DOI

[J29]. William Fornaciari, Paolo Gubian, Donatella Sciuto, Cristina Silvano, "Power Estimation of Embedded Systems: a Hardware/Software Co-design Approach", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems,** Vol.6, No. 2, Jun. 1998, pp. 266-275, DOI. This work has been selected to be re-published as Chapter 3 of the book: "Readings in Hardware/Software Co-design", Edited by G. De Micheli, R. Ernst, and W. Wolf, The Morgan Kaufmann Series in Systems on Silicon, Jun. 2001, ISBN 1-55860-702-1.

[J30]. William Fornaciari, Paolo Gubian, Donatella Sciuto, Cristina Silvano, "A VHDL-based Approach for Power Estimation of Embedded Systems", **Journal of System Architecture: The Euromicro Journal,** Volume 44, Issue 1, October 1997, pp. 37-61, DOI

[J31]. Luca Penzo, Donatella Sciuto, Cristina Silvano, "Construction Techniques for Systematic SEC-DED Codes with Single Byte Error Detection and Partial Correction Capability for Computer Memory Systems", **IEEE**

Transactions on Information Theory, Vol. 41, No. 2, Mar. 1995, pp. 584-591, DOI

5.2. INTERNATIONAL BOOKS

[B1]. Authors: Amir H. Ashouri, Gianluca Palermo, John Cavazos, Cristina Silvano **(Authors).** "Automatic Tuning of Compilers using Machine Learning", Series: PoliMI SpringerBriefs. Springer, 1st Edition, 2018, XVII, 118 p., 23 illus., 6 illus. in color, ISBN: 978-3-319-71488-2. **Book Metrics: 1059 chapter downloads** since eBook online publication on SpringerLink in 2018**.**

[B2]. Michael Huebner, Cristina Silvano, **(Editors),** "Near Threshold Computing. Technology, Methods and Applications", Springer, 1st Edition, 2016, IX, 100 p. 56 illus., Hardcover ISBN: 978-3-319-23388-8. **Book Metrics: 2 473 chapter downloads** since eBook online publication on SpringerLink in 2015.

[B3]. Cristina Silvano; Marcello Lajolo; Gianluca Palermo; **(Editors),** "Low-Power Networks-on-Chip", Springer, 1st Edition., 2011, X, 300 p. 100 illus., Hardcover ISBN: 978-1-4419-6910-1. **Book Metrics: 8 202 chapter downloads** since eBook online publication on SpringerLink in 2010.

[B4]. Cristina Silvano; William Fornaciari; Eugenio Villar; **(Editors),** "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Springer, 1st Edition, 2011, XVIII, 222, p. 88 illus. Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011. **Book Metrics: 4 041 chapter downloads** since eBook online publication on SpringerLink in 2011.

[B5]. Vittorio Zaccaria, Mariagiovanna Sami, Donatella Sciuto, Cristina Silvano **(Authors),** "Power Estimation and Optimization Methodologies for VLIW-Based Embedded Systems", Kluwer Academic Publishers, Boston, Hardbound, ISBN 1-4020-7377-1, February 2003, 201 pp.

5.3. EDITORIAL CONTRIBUTIONS

[E1]. Joao Cardoso, Cristina Silvano **(Guest Co-Editors),** Introduction to Special Section on FPL 2015, The 25th International Conference on Field Programmable Logic and Applications, ACM Transactions on Reconfigurable Technology and Systems (TRETS), Volume 10, No. 2, Article 10, 2017.

[E2]. Jeronimo Castrillon Mazo, Cristina Silvano **(Guest Co-Editors),** Guest Editorial: Special Issue on Virtual Prototyping of Parallel and Embedded Systems (ViPES), ACM Transactions on Embedded Computing Systems (TECS). Volume 16, No. 1, 2016.

[E3]. Cristina Silvano, Walter Stechele, Stephan Wong, Jerónimo Castrillón, Michael Hübner, Amir Hossein Ashouri **(Editors),** Proceedings of the 1st International Workshop on RESource Awareness and Application Auto-tuning in Adaptive and heterogeNeous compuTing, co-located with 19th International Conference on Design, Automation And Test In Europe (DATE 2016), Dresden, Germany, March 18th, 2016. Series CEUR Workshop Proceedings, Vol. 1643, CEUR-WS.org Publisher, 2016, URL

[E4]. Cristina Silvano, João M. P. Cardoso, Giovanni Agosta, Michael Hübner **(Editors),** Proceedings of the 7th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and the 5th Workshop on Design Tools and Architectures For Multicore Embedded Computing Platforms, PARMA-DITAM 2016, Prague, Czech Republic, January 18, 2016. ACM 2016, ISBN 978-1-4503-4052-6, DOI

[E5]. Peter Y. K. Cheung, Wayne Luk and Cristina Silvano **(Editors),** Preface, 25th International Conference on Field Programmable Logic and Applications, FPL 2015, London, United Kingdom, September 2-4, 2015, pages 1-2, DOI 10.1109/FPL.2015.7293746.

[E6]. Diana Göhringer, Michael Hübner, Jerónimo Castrillón, Cristina Silvano **(Editors),** ViPES 2015, Preface, 2015 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS) 2015, Samos, Greece, July 19-23, 2015: pp. 347, DOI.

[E7]. Giovanni Agosta, Cristina Silvano, João M. P. Cardoso, Michael Hübner **(Editors),** Proceedings of the 6th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and the 4th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms, PARMA-DITAM 2015, Amsterdam, Netherlands, January 21, 2015. ACM 2015, ISBN 978-1-4503-3343-6, DOI.

[E8]. Cristina Silvano, João M. P. Cardoso, Michael Hübner **(Editors),** Proceedings of the 5th Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and the 3rd Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms, PARMA-DITAM 2014, Vienna, Austria, January 20, 2014. ACM 2014, ISBN 978-1-4503-2607-0, DOI.

[E9]. Smail Niar and Cristina Silvano **(Guest Co-Editors),** Special Issue DSD 2012 on Reliability and dependability in MPSoC Technologies, Journal on Microprocessors and Microsystems - Embedded Hardware Design, Vol. 37, Number 8-A, 2013, page 759, DOI

[E10]. Daniel Gracia Pérez, Smaïl Niar, Cristina Silvano, Morteza Biglari-Abhari **(Editors):** Proceedings of the 2012 Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, RAPIDO '12, 23 January, 2012, Paris, France. ACM 2012, ISBN 978-1-4503-1114-4

[E11]. Cristina Silvano, Koen Bertels, Michael Schulte **(Guest Co-Editors),** Special Issue with selected papers from International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS2009) on Transactions on High-Performance Embedded Architectures and Compilers (Transactions on HiPEAC), Volume 5, Issue 3, Springer.

[E12]. Mladen Berekovic; William Fornaciari; Uwe Brinkschulte; Cristina Silvano; **(Editors),** "Architecture of Computing Systems - ARCS 2011", 24th International Conference, Lake Como, Italy, February 24-25, 2011. Proceedings, Springer, Series: Lecture Notes in Computer Science, Vol. 6566, Subseries: Theoretical Computer Science and General Issues, 1st Edition., 2011, XIII, 271 p., ISBN 978-3-642-19136-7.

[E13]. **Selection Committee Member,** IEEE MICRO Special Issue on "Top Picks 2010 from Computer Architecture Conferences", January/February 2011.

[E14]. Koen Bertels; Nikita Dimopoulos; Cristina Silvano; Stephan Wong; **(Editors),** Embedded Computer Systems: Architectures, Modeling, and Simulation 9th International Workshop, SAMOS 2009, Samos, Greece, July 20-23, 2009, Springer Proceedings Series: Lecture Notes in Computer Science Subseries: Theoretical Computer Science and General Issues , Vol. 5657, 2009, XIV, 342 p., Softcover ISBN: 978-3-642-03137-3.

[E15]. Paolo Faraboschi, Steve Keckler, Antonio Gonzales, Cristina Silvano; **(Editors)** Proceedings of MICRO-41 2008 41st IEEE/ACM International Symposium on Microarchitecture, 2008, 8-12 Nov. 2008, Lake Como.

5.4. CHAPTERS IN INTERNATIONAL BOOKS WITH PEER REVIEW

[CH1]. Ioannis Stamelakos, Sotirios Xydis, Gianluca Palermo, Cristina Silvano, "Variability-Aware Voltage Island Management for Near-Threshold Computing with Performance Guarantees", pp. 35-53, Near Threshold Computing. Technology, Methods and Applications, Editors: Michael Huebner, Cristina Silvano. Springer, 1st Edition., 2016, IX, 100 p. 56 illus., Hardcover ISBN: 978-3-319-23388-8.

[CH2]. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-Couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao and T. Shibin, "MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures", pp. 47-63, in "VLSI 2010 Annual Symposium", Selected Papers, Nikolaos Voros, Amar Mukherjee, Nicolas Sklavos, Konstantinos Masselos, Michael Huebner (Editors), Lecture Notes in Electrical Engineering, Volume 105, 1st Edition., 2011, VIII, 331 p., Springer Netherlands, ISBN 978-94-007-1487-8, Due: August 31, 2011, DOI: 10.1007/978-94-007-1488-5_19, url

[CH3]. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Melpignano, J.-M. Zins, D. Siorpaes, H. Hübert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Leupers, H. Meyr, J. Ansari, P. Mähönen and B. Vanthournout, "2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-Core Architectures", pp. 65-79, in "VLSI 2010 Annual Symposium", Selected Papers, Nikolaos Voros, Amar Mukherjee, Nicolas Sklavos, Konstantinos Masselos, Michael Huebner (Editors), Lecture Notes in Electrical Engineering, Volume 105, 1st Edition., 2011, VIII, 331 p., Springer Netherlands, ISBN 978-94-007-1487-8, Due: August 31, 2011, DOI: 10.1007/978-94-007-1488-5_19, url

[CH4]. C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, S. Bocchio, R. Zafalon, P. Avasare, G. Vanmeerbeeck, C. Ykman-Couvreur, M. Wouters, C. Kavka, L. Onesti, A. Turco, U. Bondi, G. Mariani, H. Posadas, E. Villar, C. Wu, F. Dongrui, Z. Hao, "The MULTICUBE Design Flow", pp. 3-17, in "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Cristina Silvano; William Fornaciari; Eugenio Villar; (Editors); Springer, 1st Edition., 2011, XVIII, 222 p., 88 illus. Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011, DOI: 10.1007/978-1-4419-8837-9, url

[CH5]. E. Rigoni, C. Kavka, A. Turco, G. Palermo, C. Silvano, V. Zaccaria, G. Mariani, "Optimization Algorithms for Design Space Exploration of Embedded Systems", pp. 51-74, in "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Cristina Silvano; William Fornaciari;

Eugenio Villar; (Editors); Springer, 1st Edition., 2011, XVIII, 222 p., 88 illus. Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011, DOI: 10.1007/978-1-4419-8837-9, url

[CH6]. G. Palermo, C. Silvano, V. Zaccaria, E. Rigoni, C. Kavka, A. Turco and G. Mariani, "Response Surface Modeling for Design Space Exploration of Embedded Systems", pp. 75-92, in "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Cristina Silvano; William Fornaciari; Eugenio Villar; (Editors); Springer, 1st Edition., 2011, XVIII, 222 p., 88 illus. Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011, DOI: 10.1007/978-1-4419-8837-9, url

[CH7]. P. Avasare, C. Ykman-Couvreur, G. Vanmeerbeeck, G. Mariani, G. Palermo, C. Silvano and V. Zaccaria, "Design Space Exploration Supporting Run-Time Resource Management", pp. 93-107, in "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Cristina Silvano; William Fornaciari; Eugenio Villar; (Editors); Springer, 1st Edition., 2011, XVIII, 222 p., 88 illus. Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011, DOI: 10.1007/978-1-4419-8837-9, url

[CH8]. C. Kavka, L. Onesti, E. Rigoni, A. Turco, S. Bocchio, F. Castro, G. Palermo, C. Silvano, V. Zaccaria, G. Mariani, F. Dongrui, Z. Hao, and T. Shibin, "Design Space Exploration of Parallel Architectures", pp. 171-188, in "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Cristina Silvano; William Fornaciari; Eugenio Villar; (Editors); Springer, 1st Edition., 2011, XVIII, 222 p., 88 illus. Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011, DOI: 10.1007/978-1-4419-8837-9, url

[CH9]. G. Mariani, C. Ykman-Couvreur, P. Avasare, G. Vanmeerbeeck, G. Palermo, C. Silvano and V. Zaccaria, "Design Space Exploration for Run-Time Management of a Reconfigurable System for Video Streaming", pp. 189-204, in "Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, The MULTICUBE Approach", Cristina Silvano; William Fornaciari; Eugenio Villar; (Editors); Springer, 1st Edition., 2011, XVIII, 222 p., 88 illus. Hardcover, ISBN 978-1-4419-8836-2, Due: August 29, 2011, DOI: 10.1007/978-1-4419-8837-9, url

[CH10]. L. Fiorin, G. Palermo, C. Silvano and M. Sami, "Security in Networks-on-Chips", pp. 123-154; in "Networks-on-Chips: Theory and Practice". Fayez Gebali, Haytham Elmiligi, and M.Watheq El-Kharashi (Eds.), Taylor & Francis Group LLC - CRC Press, US, 2009, ISBN: 978-1-4200-7978-4 (Hardcover), url

[CH11]. G. Beltrame, D. Sciuto, and C. Silvano, "A Power-Efficient Methodology for Mapping Applications on Multi-Processor System-On-Chip Architectures", pp. 177-196, VLSI-SoC: Research Trends in VLSI and Systems on Chip, Fourteenth International Conference on Very Large Scale Integration of System on Chip (VLSI-SoC2006), October 16-18, 2006, Nice, France, Series: IFIP International Federation for Information Processing , Vol. 249, Giovanni De Micheli; Salvador Mir; Ricardo Reis, (Eds.), Springer, 2008, 398 p., Hardcover ISBN: 978-0-387-74908-2, ISSN: 1571-5736, DOI and url

[CH12]. L. Benini, G. De Micheli, E. Macii, D. Sciuto, and C. Silvano, "Address Bus Encoding Techniques for System-Level Power Optimization", pp. 275-289; in **Design, Automation, and Test in Europe - The Most Influential Papers of 10 Years DATE,** Rudy Lauwereins; Jan Madsen (Eds.); 2008, 516 p., ISBN: 978-1-4020-6487-6, Springer Ed, DOI: .10.1007/978-1-4020-6488-3_6, url. This chapter represents a **re-publication** of the paper [C82].

[CH13]. D. Barretta, L. Breveglieri, P. Maistri, M. Monchiero, L. Negri, A. Pagni, G. Palermo, M. Sami, C. Silvano, O. Villa, R. Zafalon, "Low Power Architectures for Mobile Systems", pp 177-206, in "Mobile Information Systems - Infrastructure and Design for Adaptivity and Flexibility". Barbara Pernici Editor, Springer, 2006, XVI, 354p., 137 illus., ISBN 978-3-540-31008-2, url

[CH14]. W. Fornaciari , P. Gubian, D. Sciuto, C. Silvano, "Power Estimation of Embedded Systems: a Hardware/Software Co-design Approach", pp. 249-258, in "Readings in Hardware/Software Co-design", Edited by G. De Micheli, R. Ernst, e W. Wolf, The Morgan Kaufmann Series in Systems on Silicon, Kluwer Academic Publishers, Norwell, MA, USA, June, 2001, ISBN 1-55860-702-1; url. This chapter represents a **re-publication** of the journal paper appeared as [J29].

5.5. ACADEMIC TEXTBOOKS (IN ITALIAN)

1. F. Fummi, M. Sami, C. Silvano, "Progettazione digitale" (in Italian) - Second Edition, McGraw-Hill, Jan 2007, ISBN:: 88-386-6352-1, 390pp. url
2. F. Fummi, M. Sami, C. Silvano, "Progettazione digitale", (in Italian), McGraw-Hill, Feb. 2002, ISBN 88-386-6027-1.

5.6. INTERNATIONAL CONFERENCES AND WORKSHOPS WITH PEER REVIEW

[C1]. Davide Gadioli, Ricardo Nobre, Pedro Pinto, Emanuele Vitali, Amir H. Ashouri, Gianluca Palermo, Joao Cardoso, Cristina Silvano: "SOCRATES – A Seamless Online Compiler and System Runtime AutoTuning Framework for Energy-Aware Applications" *in Proceedings of* ***DATE 2015*** - International Conference on Design, Automation and Test in Europe, Dresden, 19-23 March 2018, pp. 1143-1146.

[C2]. Ioannis S. Stamelakos, Sotirios Xydis, Gianluca Palermo, Cristina Silvano: "Throughput balancing for energy efficient near-threshold manycores". The 26th International Workshop on Power and Timing Modeling, Optimization and Simulation, **PATMOS 2016,** Bremen, Germany, September 21-23, 2016: pp. 64-69, DOI

[C3]. Ioannis S. Stamelakos, Amin Khajeh, Ahmed M. Eltawil, Gianluca Palermo, Cristina Silvano, Fadi J. Kurdahi, "A System-Level Exploration of Power Delivery Architectures for Near-Threshold Manycores Considering Performance Constraints", IEEE Computer Society Annual Symposium on VLSI (**ISVLSI**) 2016, Pittsburgh, PA, USA, July 11-13, 2016, pp. 484-489, DOI

[C4]. Cristina Silvano, Giovanni Agosta, Stefano Cherubin, Davide Gadioli, Gianluca Palermo, Andrea Bartolini, Luca Benini, Jan Martinovic, Martin Palkovic, Katerina Slaninová, João Bispo, João M. P. Cardoso, Rui Abreu, Pedro Pinto, Carlo Cavazzoni, Nico Sanna, Andrea R. Beccari, Radim Cmar, Erven Rohou: "The ANTAREX approach to autotuning and adaptivity for energy efficient HPC systems". ACM Int. Conference on Computing Frontiers, **CF'2016,** Como, Italy, May 16-19, 2016: 288-293, DOI

[C5]. Cristina Silvano, Giovanni Agosta, Andrea Bartolini, Andrea Beccari, Luca Benini, João Bispo, João M. P. Cardoso, Carlo Cavazzoni, Radim Cmar, Jan Martinovic, Gianluca Palermo, Martin Palkovic, Pedro Pinto, Erven Rohou, Nico Sanna, and Katerina Slaninova, "AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems: The ANTAREX Approach", Proceedings of **DATE 2016** - IEEE/ACM Design and Test in Europe Conference, Dresden (Germany), March 14-18, 2016, pp. 708-713. DOI

[C6]. Davide Gadioli, Gianluca Palermo, Cristina Silvano, "Application Autotuning to Support Runtime Adaptivity in MulticoreArchitectures", Proceeding of XV International Conference on Systems, Architectures, Modeling, and Simulation, **IC-SAMOS 2015.** Agios Konstantinos, Samos, Greece, July 20-23, 2015, pp. 173-180. DOI

[C7]. Edoardo Paone, Francesco Robino, Gianluca Palermo, Vittorio Zaccaria, Ingo Sander and Cristina Silvano, "Customization of OpenCL Applications for Efficient Task Mapping under Heterogeneous Platform Constraints", In Proceedings of **DATE 2015** - International Conference on Design, Automation and Test in Europe. Grenoble, France. 9-13 March 2015. pp. 736-741. DOI

[C8]. Amir Hossein Ashouri, Giovanni Mariani, Gianluca Palermo and Cristina Silvano, "A Bayesian Network Approach for Compiler Auto-tuning for Embedded Processors", **ESTIMedia 2014,** The 12th IEEE Symposium on Embedded Systems for Real-time Multimedia, New Delhi, India, October 16-17, 2014. DOI

[C9]. Davide Gadioli, Simone Libutti, Giuseppe Massari, Edoardo Paone, Michele Scandale, Patrick Bellasi, Gianluca Palermo, Vittorio Zaccaria, Giovanni Agosta, William Fornaciari, and Cristina Silvano. "OpenCL Application Auto-Tuning and Run-Time Resource Management for Multi-Core Platforms" Proceeding of 12th IEEE International Symposium on Parallel and Distributed Processing with Applications, **ISPA 2014,** Milan, Italy, August 26-28, 2014, pp. 127-133. DOI

[C10]. Giuseppe Massari, Edoardo Paone, Patrick Bellasi, Gianluca Palermo, Vittorio Zaccaria, William Fornaciari, and Cristina Silvano. "Combining Application Adaptivity and System-wide Resource Management on Multi-Core Platforms", Proceeding of XIVth International Conference on Systems, Architectures, Modeling, and Simulation, **IC-SAMOS 2014.** Agios Konstantinos, Samos, Greece, July 14-17, 2014, pp. 26-33. DOI

[C11]. Edoardo Paone, Davide Gadioli, Gianluca Palermo, Vittorio Zaccaria, and Cristina Silvano. "Evaluating Orthogonality between Application Auto-Tuning and Run-Time Resource Management for Adaptive OpenCL Applications", Proceeding of IEEE 25th International Conference on Application-Specific Systems, Architectures and Processors, **ASAP 2014,** Zurich, Switzerland, June 18-20, 2014, pp. 161-168. DOI

[C12]. Giuseppe Massari, Edoardo Paone, Michele Scandale, Patrick Bellasi, Gianluca Palermo, Vittorio Zaccaria, Giovanni Agosta, William Fornaciari, Cristina Silvano: "Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures". Proceedings of Reconfigurable Computing: Architectures, Tools, and Applications - 10th International Symposium, **ARC 2014,** Vilamoura, Portugal, April 14-16, 2014. Lecture Notes in Computer Science Vol. 8405, 2014. pp. 345-352. DOI

[C13]. Cristina Silvano, Gianluca Palermo, Sotirios Xydis and Ioannis Stamelakos. “Voltage Island Management in Near Threshold Manycore Architectures to Mitigate Dark Silicon” In Proceedings of **DATE 2014** - Conference on Design, Automation and Test in Europe. Dresden, Germany. 24-28 March 2014, pp. 1-6. DOI

[C14]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. “DeSpErate: Speeding-up Design Space Exploration by using Predictive Simulation Scheduling”. In Proceedings of **DATE 2014** - Conference on Design, Automation and Test in Europe. Dresden, Germany. 24-28 March 2014, pp. 1-4. DOI

[C15]. Giovanni Mariani, Gianluca Palermo, Roel Meeuws, Vlad-Mihai Sima, Cristina Silvano and Koen Bertels. “DRuiD: Designing Reconfigurable Architectures with Decision-making Support”, In Proceedings of **ASP-DAC 2014,** 19th Asia and South Pacific Design Automation Conference. Singapore. January 20-23, 2014, pp. 213-218. DOI

[C16]. Ioannis S. Stamelakos, Sotirios Xydis, Gianluca Palermo and Cristina Silvano. “Variation Aware Voltage Island Formation for Power Efficient Near-Threshold Manycore Architectures”, In Proceedings of **ASP-DAC 2014,** 14th Asia and South Pacific Design Automation Conference. Singapore. January 20-23, 2014, pp. 304-310. DOI

[C17]. Amir Hossein Ashouri, Vittorio Zaccaria, Sotirios Xydis, Gianluca Palermo and Cristina Silvano " A Framework for Compiler Level Statistical Analysis over Customized VLIW Architecture ", In **VLSI-SoC 2013** - International Conference on Very Large Scale Integration and System-on-Chip Istanbul, Turkey. 7-9 October 2013, pp. 124-129. DOI

[C18]. Giovanni Mariani, Vlad-Mihai Sima, Gianluca Palermo, Vittorio Zaccaria, Giacomo Marchiri, Cristina Silvano and Koen Bertels. "Run-time Optimization of a Dynamically Reconfigurable Embedded System Through Performance Prediction ", In **FPL 2013** – 23rd International Conference on Field Programmable Logic and Applications. Porto, Portugal. 2-4 September 2013, pp. 1-8, DOI

[C19]. Sotirios Xydis, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "A Meta-Model Assisted Coprocessor Synthesis Framework for Compiler/Architecture Parameters Customization", In **DATE 2013** - International Conference on Design, Automation and Test in Europe. Grenoble, France. March 18-22, 2013, pp. 659-664, url

[C20]. Edoardo Paone, Nazanin Vahabi, Vittorio Zaccaria, Cristina Silvano, Diego Melpignano, Germain Haugou, Thierry Lepley, "Improving Simulation Speed and Accuracy for Many-Core Embedded Platforms with Ensemble Models", In **DATE 2013** - International Conference on Design, Automation and Test in Europe. Grenoble, France. March 18-22, 2013, pp. 671-676. url

[C21]. Sotirios Xydis, Gianluca Palermo, Cristina Silvano. "Thermal-Aware Datapath Merging for Coarse-Grained Reconfigurable Processors", In **DATE 2013** - International Conference on Design, Automation and Test in Europe. Grenoble, France. March 18-22, 2013, pp. 1649-1654, url

[C22]. Edoardo Paone, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, Diego Melpignano, Germain Haugou and Thierry Lepley, "An Exploration Methodology for a Customizable OpenCL Stereo-Matching Application Targeted to an Industrial Multi-Cluster Architecture", in Proceedings of the 8th IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis, **CODES+ISSS 2012,** 7-12 October 2012, Tampere, Finland. Pp. 503-512, ACM, New York, USA, ISBN: 978-1-4503-1426-8, DOI

[C23]. Debora Matos, Gianluca Palermo, Cezar Reinbrecht, Cristina Silvano, Altamiro Amadeu Susin, Luigi Carro. "Floorplan-Aware Hierarchical NoC Topology with GALS Interfaces "In Proceedings of **ISCAS 2012** - IEEE International Symposium on Circuits and Systems. Seoul, Korea. 20-23 May 2012, pp. 652-655. ISBN: 9781467302197, ISSN: 0271-4302, DOI

[C24]. Giovanni Mariani, Vlad Mihai Sima, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano, Koen Bertels. "Using multi-objective design space exploration to enable run-time resource management for reconfigurable architectures", In Proceedings of the Conference on Design, Automation and Test in Europe (**DATE 2012**). Dresden, Germany. 12-16 March 2012, pp. 1379-1384, **ISBN:** 978-1-4577-2145-8, url

[C25]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "Evaluating Run-time Resource Management Policies for Multi-core Embedded Platforms with the EMME Evaluation Framework. ", In **ARCS 2012 Workshops**, 2PARMA Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures. Munich, Germany. Feb. 2012 pp. 363-374. url

[C26]. Debora Matos, Gianluca Palermo, Vittorio Zaccaria, Cezar Reinbrecht, Altamiro Susin, Cristina Silvano and

Luigi Carro, "Floorplanning-Aware Design Space Exploration for Application-Specific Hierarchical Networks on-Chip", In **NoCArc'11** - Fourth International Workshop on Network on-Chip Architectures. In conjunction with the 44th Annual IEEE/ACM Int. Symposium on Microarchitecture (MICRO-44) December 3-7, 2011 Porto Alegre, Brazil, ISBN: 9781450309479, DOI:

[C27]. Caroline Concatto, Anelise Kologeski, Luigi Carro, Fernanda Kastensmidt, Gianluca Palermo, Cristina Silvano. "Two-levels of adaptive buffer for virtual channel router in NoCs", In Proceedings of IEEE/IFIP 19th International Conference on VLSI and System-on-Chip (**VLSI-SoC 2011**), Kowloon, Hong Kong, China, Oct. 3-5, 2011, pp. 302-307. ISBN: 978-1-4577-0171-9 DOI

[C28]. Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "ARTE: an Application-specific Run-Time Management Framework for Multi-core Systems" In Proceedings of the IEEE 9th Symposium on Application Specific Processors (**SASP2011**), San Diego, CA, USA, 5-6 June 2011, pp. 86-93. IEEE Computer Society, Washington, DC, USA, ISBN: 9781457712128, DOI

[C29]. Leandro Fiorin, Gianluca Palermo, Cristina Silvano. "A Monitoring System for NoCs ", in Proceedings of the Third International Workshop on Network on Chip Architectures, **NoCArc '10,** 2010, ISBN 978-1-4503-0397-2, Atlanta, Georgia, pp. 25--30. In Conjunction with the 43rd Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-43, ACM, New York, NY, USA, 25-30. DOI

[C30]. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Aleksandar Brankovic, Jovana Jovic, Cristina Silvano. "A Correlation-Based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip ", In Proceedings of the 47th Design Automation Conference. Design Automation Conference (**DAC-47)**, Anaheim, CA, USA, 13-18 June 2010, pp. 120-125, New York, NY, USA, ACM/IEEE , ISBN: 9781450300025, DOI **HiPEAC 2010 Paper Award**

[C31]. Giovanni Mariani, Vittorio Zaccaria, Gianluca Palermo, Prabhat Avasare, Geert Vanmeerbeeck, Chantal Ykman-Couvreur, Cristina Silvano, "An industrial design space exploration framework for supporting run-time resource management on multi-core systems ", In Proceedings of the Conference on Design, Automation and Test in Europe (**DATE 2010**). Dresden, Germany. March 2010, pp. 196-201. EDAA, Leuven, Belgium, Belgium, ISBN: 978-1-4244-7054-9, url

[C32]. Arpad Gellert, Gianluca Palermo, Vittorio Zaccaria, Adrian Florea, Lucian Vintan, Cristina Silvano. " Energy-Performance Design Space Exploration of SMT Architectures Exploiting Selective Load Value Predictions ", In Proceedings of the Conference on Design, Automation and Test in Europe (**DATE 2010**). Dresden, Germany. March 2010, pp. 271-274. EDAA, Leuven, Belgium, Belgium, ISBN: 978-1-4244-7054-9, url

[C33]. Vittorio Zaccaria, Gianluca Palermo, Giovanni Mariani, Fabrizio Castro, Cristina Silvano. "Multicube Explorer: An Open Source Framework for Design Space Exploration of Chip Multi-Processors ", In **ARCS2010 Workshops,** PARMA Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures, co-located with ARCS 2010, Hannover, Germany, February 2010, pp. 325-331. VDE Verlag, ISBN: 978-3-8007-3222-7 url

[C34]. Anirban Dutta Choudhury, Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "Yield Enhancement by Robust Application-specific Mapping on Network-on-Chips ", In **NoCArc'09** - Second International Workshop on Network on-Chip Architectures, in Conjunction with the 42nd Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-42, New York City, USA, December 2009, pp. 37-42.

[C35]. Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "Meta-model Assisted Optimization for Design Space Exploration of Multi-Processor Systems-on-Chip ", In Euromicro Proceedings of **DSD'09** - Conference on Digital System Design. Patras, Greece, August 2009, pp. 383-389. ISBN: 9780769537825, DOI: 10.1109/DSD.2009.154

[C36]. Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "A Design Space Exploration Methodology Supporting Run-Time Resource Management for Multi-Processors Systems-on-Chip", In Proceedings of the IEEE 7th Symposium on Application Specific Processors, **SASP 2009**, Co-located with DAC 2009, San Francisco, CA, USA, 27-28 July 2009, pp. 21-28, ISBN: 978-1-4244-4939-2, DOI

[C37]. Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "Multiprocessor System-on-Chip Design Space Exploration based on Multi-level Modeling Techniques", In Proceedings of **IC-SAMOS'09** – IEEE International Conference on Embedded Computer Systems: Architectures, MOdeling, and Simulation, Samos, Greece, July 2009, pp. 118-124. ISBN: 9781424445011, doi: 10.1109/ICSAMOS.2009.5289222.

[C38]. Leandro Fiorin, Gianluca Palermo, Cristina Silvano. "MPSoCs Run-Time Monitoring through Networks-on-

Chip", In **DATE 2009** - International Conference on Design, Automation and Test in Europe. Nice, France. April 2009, pp. 558-561. ISBN: 9781424437818.

[C39]. G. Palermo C. Silvano, V. Zaccaria, "Variability-Aware Robust Design Space Exploration of Chip Multiprocessor Architectures". In Proceedings of **ASP-DAC 2009,** 14th Asia and South Pacific Design Automation Conference. Yokohama, Japan, January 2009, pp. 323-328. ISBN: 9781424427482, DOI: 10.1109/ASPDAC.2009.4796501.

[C40]. L. Fiorin, G. Palermo, C. Silvano, "A Security Monitoring Service for NoCs", In ACM Proceedings of **CODES+ISSS 2008** - International Conference on Hardware-Software Codesign and System Synthesis. Atlanta, Georgia, USA, October 2008, pp. 197-2002.

[C41]. G. Palermo, C. Silvano, V. Zaccaria, "Robust Optimization of SoC Architectures: A Multi-Scenario Approach", In Proceedings of **ESTIMedia 2008** - IEEE Workshop on Embedded Systems for Real-Time Multimedia. Atlanta, Georgia, USA, October 2008, pp. 7-12.

[C42]. O. Villa, G. Palermo, C. Silvano, "Efficiency and Scalability of Barrier Synchronization on NoC Based Many-core Architectures", In Proceedings of **CASES 2008** - International Conference on Compilers, Architectures and Synthesis for Embedded Systems. Atlanta, Georgia, USA, October 2008, pp. 81-90.

[C43]. G. Mariani, G.Palermo, C. Silvano and V. Zaccaria, "An Efficient Design Space Exploration Methodology for Multi-Cluster VLIW Architectures based on Artificial Neural Networks", **IFIP-VLSI-SOC 2008,** 2008 IFIP International Conference on Very Large Scale Integration, 13-15 Oct. 2008, Rhodos (Greece).

[C44]. G.Palermo, C. Silvano and V. Zaccaria, "Discrete Particle Swarm Optimization for Multi-objective Design Space Exploration", Proceedings of 11th IEEE Euromicro Conference on Digital System Design Architectures, Methods and Tools (**DSD 2008,** 2008, Sept. 2-5, Parma, Italy.

[C45]. M. Monchiero, G. Palermo, C. Silvano, O. Villa, "A Modular Approach to Model Heterogeneous MPSoC at Cycle Level", Proceedings of 11th IEEE Euromicro Conference on Digital System Design Architectures, Methods and Tools (**DSD 2008**), 2008, Sept. 2-5, Parma, Italy.

[C46]. G. Palermo, C. Silvano e V. Zaccaria, "An Efficient Design Space Exploration Methodology for Multiprocessor SoC Architectures based on Response Surface Methods", **SAMOS VIII:** International Symposium on Systems, Architectures, MOdeling and Simulation, Samos, Greece, July 21-24, 2008.

[C47]. G. Palermo, C. Silvano e V. Zaccaria, "An Efficient Design Space Exploration Methodology for On-Chip Multiprocessors Subject to Application-Specific Constraints", IEEE Symposium on Application Specific Processors (**SASP 2008**), Co-located with DAC 2008, 8-9 June 2008, Anaheim (CA - USA), pp.75-82.

[C48]. Martino Sykora, Giovanni Agosta and Cristina Silvano, “Dynamic Configuration of Application-Specific Implicit Instructions for Embedded Pipelined Processors”, pp. 1509-1516, in Proceedings of the 2008 ACM Symposium on Applied Computing **(SAC2008),** Fortaleza, Ceara, Brazil, March 16-20, 2008. ISBN: 978-1-59593-753-7, Roger L. Wainwright and Hisham Haddad (Editors) DOI **ACM BEST PAPER AWARD SAC2008 - Applications Theme**.

[C49]. G. Palermo, G. Mariani, C. Silvano, R. Locatelli, M. Coppola, "A Topology Design Customization Approach for STNoC", In Proceedings of **NanoNets'07** - International Conference on NanoNetworks. Catania, Italy, Sept. 2007.

[C50]. L. Fiorin, G. Palermo, S. Lukovic, C. Silvano, "A Data Protection Unit for NoC-based Architectures", **CODES+ISSS '07:** Proceedings of the 5th IEEE/ACM International Conference on Hardware/software Codesign and System Synthesis, Salzburg, Austria, 2007, pp. 167--172.

[C51]. G. Palermo, G. Mariani, C. Silvano, R. Locatelli, M. Coppola, "Application-Specific Topology Design Customization for STNoC", Proceedings of 10th IEEE Euromicro Conference on Digital System Design Architectures, Methods and Tools (**DSD 2007**), 2007, Lübeck, Germany, pp. 547-550.

[C52]. Leandro Fiorin, Cristina Silvano, Mariagiovanna Sami, "Security Aspects in Networks-on-Chips: Overview and Proposals for Secure Implementations", Proceedings of 10th IEEE Euromicro Conference on Digital System Design Architectures, Methods and Tools (**DSD 2007**), 2007, Lübeck, Germany, pp. 539-542.

[C53]. G. Palermo, G. Mariani, C. Silvano, R. Locatelli, M. Coppola, "Mapping and Topology Customization Approaches for Application-Specific STNoC Designs", In Proc. of **ASAP'07** - 18th IEEE International Conference on Application-specific Systems, Architectures and Processors. Montréal, Québec, Canada, July 2007, pp. 61-68.

[C54]. G. Beltrame, D. Bruschi, D. Sciuto, C. Silvano, "Decision-theoretic Exploration of Multi-Processor Platforms", **CODES+ISSS 2006,** in Proceedings of the 4th International Conference on Hardware/Software

Codesign and System Synthesis, Seoul, Korea, October 22-25, 2006, pp. 205-210, ACM, New York, NY, USA, ISBN: 1-59593-370-0, DOI

[C55]. Beltrame G., Sciuto D., Silvano C., Paulin P., Bensoudane E., "An Application Mapping Methodology and Case Study for Multi-Processor On-Chip Architectures" **IFIP-VLSI-SOC 2006,** 2006 IFIP International Conference on Very Large Scale Integration, Publication Date: 16-18 Oct. 2006 On page(s): 146-151 ISBN: 3-901882-19-7.

[C56]. M. Monchiero, G. Palermo, C. Silvano, O. Villa, "Exploration of Distributed Shared Memory Architectures for NoC-based Multiprocessors" **IC-SAMOS VI** Conference - Embedded Computer Systems: Architectures, MOdeling, and Simulation, Samos (Greece), July 17 - 20, **2006**, pp. 144-151.

[C57]. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, and Oreste Villa, "Power/Performance Hardware Optimization for Synchronization Intensive Applications in MPSoCs", Proceedings of the Conference on Design, Automation and Test in Europe, **DATE 2006,** Munich, Germany, March 6-10, 2006, pp. 606-611. Georges G. E. Gielen Editor, European Design and Automation Association Publisher, Leuven, Belgium, ISBN: 3-9810801-0-6; DOI

[C58]. Giovanni Beltrame, Donatella Sciuto, Cristina Silvano, Damien Lyonnard and Chuck Pilkington, "Exploiting TLM and Object Introspection for System-Level Simulation", Proceedings of the Conference on Design, Automation and Test in Europe, **DATE 2006,** Munich, Germany, March 6-10, 2006, pp. 100-105. Georges G. E. Gielen Editor, European Design and Automation Association Publisher, Leuven, Belgium, ISBN: 3-9810801-0-6; DOI

[C59]. G. Beltrame, G. Palermo, D. Sciuto, C. Silvano, "Plug-in of Power Models in the StepNP Exploration Platform: Analysis of Power/Performance Trade-offs", Proceedings of the 2004 International Conference on Compilers, Architectures and Synthesis for Embedded Systems (**CASES 2004)**, Washington DC, USA, 22-25 September, 2004, pp. 85-92, ISBN:1-58113-890-3, DOI: 10.1145/1023833.1023847, DOI

[C60]. G. Palermo, C. Silvano, "PIRATE: A Framework for Power/Performance Exploration of Network-On-Chip Architectures", Proc. of **PATMOS 2004:** 14th International Workshop on Power and Timing Modeling, Optimization and Simulation, Santorini, Greece, 15-17 September, 2004, Lecture Notes in Computer Science, Springer, Vol. 3254, 2004, ISBN 978-3-540-23095-3, pp. 521-531. DOI

[C61]. M. Monchiero, G. Palermo, M. Sami, C. Silvano, V. Zaccaria, R. Zafalon, "Power-Aware Branch Prediction Techniques: A Compiler-Hints Based Approach for VLIW Processors", **GLS-VLSI'04:** Proceedings of the 14th ACM Great Lakes symposium on VLSI, April 26--28, 2004, Boston, MA, USA, pp. 440-443.

[C62]. G.Agosta, G. Palermo, C. Silvano, "Multi-Objective Co-Exploration of Source Code Transformations and Design Space Architecture for Low-Power Embedded Systems". In **SAC04:** Proceedings of the 2004 ACM Symposium on Applied Computing, 14-17 March 2004, Nicosia, Cyprus, pp. 891-896, ISBN:1-58113-812-1.

[C63]. G. Palermo, C. Silvano, V. Zaccaria, "A Flexible Framework for Fast Multi-Objective Design Space Exploration of Embedded Systems" Proc. of **PATMOS 2003**: 13th International Workshop on Power and Timing Modeling, Optimization and Simulation, September 10-12, 2003, Torino, Italy, Lecture Notes in Computer Science, Springer, Volume 2799, 2003, ISBN: 978-3-540-20074-1, pp. pp. 249 – 258.

[C64]. G. Palermo, M. Sami, C. Silvano, V. Zaccaria, R. Zafalon, "Branch Prediction Techniques for Low-Power VLIW Processors", **GLS-VLSI'03:** Proceedings of the 14th ACM Great Lakes symposium on VLSI, April 28--29, 2003, Washington, DC, USA, pp. 225-228, ISBN:1-58113-677-3.

[C65]. G. Palermo, C. Silvano, S. Valsecchi, V. Zaccaria, "A System-Level Methodology for Fast Multi-Objective Design Space Exploration", **GLS-VLSI'03:** Proceedings of the 14th ACM Great Lakes symposium on VLSI, April 28--29, 2003, Washington, DC, USA, pp. 92-95, ISBN:1-58113-677-3.

[C66]. L. Salvemini, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, and R. Zafalon, "A Methodology for the Efficient Architectural Exploration of Energy-Delay Trade-offs for Embedded Systems" **SAC03:** Proceedings of the 2003 ACM Symposium on Applied Computing, 9-12 March 2003, Melbourne, Florida, USA, pp. 672-678, ISBN:1-58113-624-2

[C67]. G. Palermo, C. Silvano, V. Zaccaria, "Power-Performance System-Level Exploration of a MicroSPARC2-based Embedded Architecture", **DATE 2003:** Design, Automation and Test in Europe, Conference and Exhibition, 03–07 Marzo 2003, Munich, GERMANY, Pages: 182-187 suppl.

[C68]. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon, "Energy Estimation and Optimization of Embedded VLIW Processors based on Instruction Clustering", **DAC2002** - ACM/IEEE Design Automation

Conference, 10-14 June, 2002, New Orleans, USA, Pages: 886-891.

[C69]. A. Bona, M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon, "An instruction-level methodology for power estimation and optimization of embedded VLIW cores", **Proc. of DATE 2002:** ACM/IEEE Design Automation and Test in Europe, Conference and Exhibition, 4-8 March, 2002, p. 1128.

[C70]. L. Benini, D. Bruni, M. Chinosi, C. Silvano, V. Zaccaria, and R. Zafalon, "A Power Modeling and Estimation Framework for VLIW-based Embedded Systems", Proc. of **PATMOS01-** IEEE Eleventh International Workshop on Power and Timing Modeling, Optimization and Simulation, Sept. 26-28, 2001, Yverdon-les-Bains, Switzerland. The paper has been selected to be re-published on: **ST Journal of System Research,** No. 0, July 2003, Art. 5, pp. 52-60.

[C71]. W. Fornaciari, D. Sciuto, C. Silvano, V. Zaccaria, "Fast System-Level Exploration of Memory Architectures Driven by Energy-Delay Metrics", **ISCAS2001:** IEEE Int. Symposium on Circuits and Systems, Sydney, Australia, May 5-7, 2001, pp.502-505, vol.4.

[C72]. W. Fornaciari, D. Sciuto, C. Silvano, V. Zaccaria, "A Design Framework to Efficiently Explore Energy-Delay Tradeoffs", **CODES-2001:** 9th ACM/IEEE International Symposium on Hardware/Software Co-Design (Former Workshop), Copenhagen (Denmark), Apr. 25-27, 2001, pp. 260-265.

[C73]. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, R. Zafalon, " Exploiting Data Forwarding to Reduce the Power Budget of VLIW Embedded Processors", **DATE2001:** IEEE Design, Automation and Test Conference in Europe, Munich, Germany, Mar. 13-16, 2001, pp. 252-257.

[C74]. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, "Power Exploration for Embedded VLIW Architectures", **ICCAD-2000:** IEEE/ACM Int. Conference on Computer Aided Design, San Jose, CA, Nov. 5-9, 2000, pp. 498-503.

[C75]. P. Bacchetta, L. Daldoss, D. Sciuto, C. Silvano, "Low-Power State Assignment Techniques for Finite State Machines", **ISCAS2000:** IEEE Int. Symposium on Circuits and Systems, Geneva (Swizerland), May 28-31, 2000, pp. 641-644, Vol. 2.

[C76]. M. Sami, D. Sciuto, C. Silvano, V. Zaccaria, "Instruction-Level Power Estimation for Embedded VLIW Cores", **CODES-2000:** 8th ACM/IEEE International Workshop on Hardware/Software Co-Design, San Diego, CA, May 3-5, 2000, pp. 34-38.

[C77]. W. Fornaciari, M. Polentarutti, D. Sciuto, C. Silvano, "Power Optimization of System-Level Address Buses based on Software Profiling", **CODES-2000:** 8th ACM/IEEE International Workshop on Hardware/Software Co-Design, San Diego, CA, May 3-5, 2000, pp. 29-33.

[C78]. W. Fornaciari, D. Sciuto, C. Silvano, "Power Estimation of System-Level Buses for Microprocessor-Based Architectures: A Case Study", IEEE International Conference on Computer Design, **ICCD-99,** Austin, TX (USA), Oct. 10-13, 1999, pp. 131-136. DOI: 10.1109/ICCD.1999.808417 url

[C79]. W. Fornaciari, D. Sciuto, C. Silvano, "Power Estimation for Architectural Exploration of HW/SW Communication on System-Level Buses", Proceedings of the Seventh International Workshop on Hardware/Software Co-Design, **CODES-99,** Rome, Italy, 3-5 May, 1999, pp. 152-156. DOI

[C80]. W. Fornaciari, D. Sciuto, C. Silvano, "Influence of Caching and Encoding on Power Dissipation of System-Level Buses for Embedded Systems", **DATE-99:** Proceedings of 1999 IEEE Conference on Design, Automation and Test in Europe, Munich (Germany), Mar. 9-12, 1999, pp. 762-763. DOI: 10.1109/DATE.1999.761219 url

[C81]. C. Guardiani, A. Macii, E. Macii, M. Poncino, M. Rossello, R. Scarsi, C. Silvano, R. Zafalon, "RTL Power Embedded Estimation in a Industrial Design Flow", IEEE Alessandro Volta Memorial Workshop on Low-Power Design, Como, Italy, Mar. 4-5, 1999, pp. 91-96. ISBN: 0-7695-0019-6, url

[C82]. D. Sciuto, C. Silvano, R. Stefanelli, "Systematic AUED Codes for Self-Checking Architectures", **DFT-98:** 1998 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Austin, TX (USA), Nov. 2-4, 1998, pp. 183-191.

[C83]. N. Dragone, C. Guardiani, C. Silvano, R. Zafalon, "Power Invariant Vector Compaction based on Bit Clustering and Temporal Partitioning", **ISLPED 1998,** IEEE International Symposium on Low-Power Electronics and Design, Monterey, CA (USA), Aug. 1998, pp. 118-120. ISBN 1-58113-059-7, DOI

[C84]. L. Daldoss, D. Sciuto, C. Silvano, "State Encoding for Low Power Embedded Controllers", **ISCAS-98:** Proceedings of 1998 IEEE International Symposium on Circuits and Systems, Monterey, CA (USA), May 31 – Jun. 3, 1998, pp. 421-424, Vol. 2. ISBN: 0-7803-4455-3 DOI

[C85]. L. Benini, G. De Micheli, E. Macii, D. Sciuto, C. Silvano, "Address Bus Encoding Techniques for System-Level Power Optimization", **DATE-98:** IEEE Design, Automation and Test in Europe, Conference an

Exhibition 1998, Paris (France), Feb. 23-26, 1998, IEEE Computer Society, ISBN: 0-8186-8359-7 pp. 861-866. DOI: 10.1109/DATE.1998.655959. url. In 2008, this paper has been recognized as one of the most influential papers of the past ten years DATE and then selected to be **re-published** as a chapter of the volume: **Design, Automation, and Test in Europe - The Most Influential Papers of 10 Years DATE** Lauwereins, Rudy; Madsen, Jan (Eds.), 2008, Approx. 250 p., ISBN: 978-1-4020-6487-6, Springer Ed.

[C86]. W. Fornaciari, P. Gubian, D. Sciuto, C. Silvano, "System-level Power Evaluation Metrics", **ISIS-97:** Second Annual IEEE International Conference on Innovative Systems in Silicon, Austin, TX (USA), Oct. 8-10, 1997, pp. 323-330. DOI: 10.1109/ICISS.1997.630275

[C87]. W. Fornaciari, P. Gubian, D. Sciuto, C. Silvano, "High-Level Power Estimation of VLSI Systems", **ISCAS-97:** Proceedings of 1997 IEEE International Symposium on Circuits and Systems, Hong Kong, Jun. 9-12, 1997, pp. 1804-1807, Vol.3. ISBN: 0-7803-3583-X, DOI

[C88]. L. Benini, G. De Micheli, E. Macii, D. Sciuto, C. Silvano, "Asymptotic Zero-Transition Activity Encoding for Address Busses in Low-Power Microprocessor-Based Systems", in **GLS-VLSI-97:** Proceedings of Seventh Great Lakes Symposium on VLSI, 1997, Urbana-Champaign, IL (USA), March 13-15, 1997, pp. 77-82, IEEE Computer Society, **ISBN:** 0-8186-7904-2 DOI . **Citation count: 360;** This paper represents **my top ranked paper** in terms of citations based on Harzing's author impact analysis and Google Scholar.

[C89]. W. Fornaciari, P. Gubian, D. Sciuto, C. Silvano, "A Conceptual Analysis Framework for Low Power Design of Embedded Systems", **ISIS-96:** 1996 Annual IEEE International Conference on Innovative Systems in Silicon (Previously: International Conference on Wafer Scale Integration), Austin, TX (USA), Oct. 9-11, 1996, pp. 170-179. DOI: 10.1109/ICISS.1996.552424

[C90]. L. Penzo, D. Sciuto, C. Silvano, "GECO: A Tool for Automatic Generation of Error Control Codes for Computer Applications", **ISCAS-95:** IEEE International Symposium on Circuits and Systems, Seattle, WA (USA), Apr. 29 – May 3, 1995, pp. 912-915.

[C91]. L. Penzo, D. Sciuto, C. Silvano, "VLSI Design of Systematic Odd-Weight-Column Byte Error Detecting SEC-DED Codes", **VLSI Design 95:** IEEE 8th International Conference on VLSI Design, New Delhi (India), Jan. 4-7, 1995, pp. 156-160. DOI: 10.1109/ICVD.1995.512096, url

[C92]. L. Populin, G. Sada, C. Silvano, "RamGen: a Dual Port Static RAM Generator", **ASIC-92:** Proceedings of Fifth Annual IEEE International ASIC Conference and Exhibit, Rochester, NY (USA), 21-25 Sept., 1992, pp. 509-512, DOI: 10.1109/ASIC.1992.270211

[C93]. F. Bozzetti, C. Silvano, "Architecture and Design Methodology of a 32-bit Microprocessor", Proc. of **COMPEURO-91:** Advanced Computer Technology, Reliable Systems and Applications, 5th Annual European Computer Conference Bologna (Italy), 13-16 May, 1991, pp. 613-617. DOI: 10.1109/CMPEUR.1991.257460

5.7. INVITED PAPERS

[IP1]. Cristina Silvano, Giovanni Agosta, Stefano Cherubin, Davide Gadioli, Gianluca Palermo, Andrea Bartolini, Luca Benini, Jan Martinovic, Martin Palkovic, Katerina Slaninová, João Bispo, João M. P. Cardoso, Rui Abreu, Pedro Pinto, Carlo Cavazzoni, Nico Sanna, Andrea R. Beccari, Radim Cmar, Erven Rohou, "The ANTAREX approach to autotuning and adaptivity for energy efficient HPC systems". **Invited Paper,** Proc. of the ACM International Conference on Computing Frontiers **CF'16,** Como, Italy, May 16-19, 2016, pp.288-293, DOI .

[IP2]. Cristina Silvano, Giovanni Agosta, Andrea Bartolini, Andrea Beccari, Luca Benini, João M. P. Cardoso, Carlo Cavazzoni, Radim Cmar, Jan Martinovic, Gianluca Palermo, Martin Palkovic, Erven Rohou, Nico Sanna, and Katerina Slaninova, "ANTAREX - AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems". **Invited Paper,** Special Session on FET-HPC and Exascale Recently EU-funded projects, 18th IEEE International Conference on Computational Science and Engineering (**CSE2015**), Porto (Portugal), pp. 343-346. DOI

[IP3]. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J. M. Zins, D. Siorpaes, H. Hübert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, H. Meyr, J. Ansari, P. Mähönen, and B. Vanthournout. "Parallel paradigms and run-time management techniques for many-core architectures: the 2PARMA approach". **Invited Paper,** *Proceedings of the 2012 Interconnection Network Architecture: On-Chip, Multi-Chip Workshop* **(INA-OCMC '12).** 25 January, 2012, Paris, France, ISBN 978-1-4503-1010-9, ACM, New York, NY, USA, pp. 39-42. DOI

[IP4]. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S.

Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Leupers H. Meyr, J. Ansari, P. Mahonen, and B. Vanthournout " Parallel Paradigms and Run-time Management Techniques for Many-core Architectures: The 2PARMA Approach ". **Invited Paper,** (**INDIN 2011**), 2011 9th IEEE International Conference on Industrial Informatics, Capariccia, Lisbon, Portugal, 26-29 July 2011, pp. 835-840. ISBN: 978-1-4577-0435-2, DOI

[IP5]. A. Bartzas, P. Bellasi, I. Anagnostopoulos, C. Silvano, W. Fornaciari, D. Soudris, D. Melpignano, C. Ykman-Couvreur, "Runtime Resource Management Techniques for Many-core Architectures: The 2PARMA Approach", **Invited Paper,** Proceedings of the 2011 Int. Conference on Engineering of Reconfigurable Systems and Algorithms (**ERSA'11**), Las Vegas, Nevada, USA, 18/07/2011 - 21/07/2011, pp. 219-230, DOI: 10.1.1.217.7368 ; url

[IP6]. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Siorpaes, H. Huebert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Leupers H. Meyr, J. Ansari, P. Mahonen, and B. Vanthournout "Parallel Programming and Run-time Resource Management Framework for Many-core Platforms: The 2PARMA Approach". **Invited Paper, ReCoSoc 2011**: 2011 6th International Workshop on Reconfigurable Communication-centric Systems-on-Chip, Montpellier, France, 20-22 June 2011, pp. 1-7. ISBN: 978-1-4577-0640-0; DOI

[IP7]. Silvano, C.; Fornaciari, W.; Palermo, G.; Zaccaria, V.; Castro, F.; Martinez, M.; Bocchio, S.; Zafalon, R.; Avasare, P.; Vanmeerbeeck, G.; Ykman-Couvreur, C.; Wouters, M.; Kavka, C.; Onesti, L.; Turco, A.; Bondi, U.; Marianik, G.; Posadas, H.; Villar, E.; Wu, C.; Fan Dongrui; Zhang Hao; Shibin, T. "MULTICUBE: Multi-objective design space exploration of multi-core architectures " **Invited Paper, ISVLSI 2010,** 2010 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 488-493, Lixouri, Kefalonia - Greece, 5-7, July 2010. ISBN: 978-1-4244-7321-2; DOI

[IP8]. Silvano, C.; Fornaciari, W.; Reghizzi, S.C.; Agosta, G.; Palermo, G.; Zaccaria, V.; Bellasi, P.; Castro, F.; Corbetta, S.; Di Biagio, A.; Speziale, E.; Tartara, M.; Siorpaes, D.; Hübert, H.; Stabernack, B.; Brandenburg, J.; Palkovic, M.; Raghavan, P.; Ykman-Couvreur, C.; Bartzas, A.; Xydis, S.; Soudris, D.; Kempf, T.; Ascheid, G.; Leupers, R.; Meyr, H.; Ansari, J.; Mähönen, P.; Vanthournout, B. "2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-core Architectures ", **Invited Paper, ISVLSI 2010,** 2010 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 494-499, Lixouri, Kefalonia - Greece, 5-7 July 2010.ISBN: 978-1-4244-7321-2; DOI

6. LIST OF PATENTS AND AWARDS

6.1. PATENTS

Inventor/Co-inventor of **11** patent applications with Bull HN Information Systems and STMicroelectronics **(7 out of 11 already granted)**:

- Integrated CMOS static RAM, EU Patent # **EP0578900 (B1)** [P1-EU] Granted 1997, DE Patent # **DE69223046 (T2)** [P1-DE] Granted 1998. Applicant: Bul HN Information Systems (IT)
- Digital information error correcting apparatus for single error correcting (SEC), double error detecting (DED), single byte error detecting (SBED), and odd numbered single byte error correcting (OSBEC), US Patent # **US5535227 (A)** [P2-US] Granted 1996. EU Patent # **EP0629051 (B1)** [P2-EU] Granted 1998, DE Patent # **DE69317766 (T2)** [P2-DE] Granted 1998. Applicant: Bul HN Information Systems (IT).
- Encoder/decoder architecture and related processing system, US Patent # **US20020019896 (A1)** [P3-US] Filed 2002. Encoder architecture for parallel busses, EU Patent # **EP1150467 (A1)** [P3-EU] Filed 2001. Applicant: ST Microelectronics (IT)
- Processor architecture US Patent # **US6889317 (B2)** [P4-US] Granted 2005. Processor architecture with variable-stage pipeline, EU Patent # **EP1199629 (A1)** [P4-EU] Filed 2002. Applicant: ST Microelectronics (IT)
- Programmable data protection device, secure programming manager system and process for controlling access to an interconnect network for an integrated circuit. US Patent # **US8185934 (B2)** [P5-US] Granted 2012. EU Patent # **EP2043324 (A1)** [P5-EU] Filed 2009. Applicant: STMicroelectronics Grenoble (F)

6.2. AWARDS AND RECOGNITIONS

- In 2017, Cristina Silvano has been elevated to the grade of **IEEE Fellow** by the IEEE Board of Directors *"for contributions to energy-efficient computer architectures"*. The IEEE Grade of Fellow is conferred by the IEEE Board of Directors upon a person with an outstanding record of accomplishments in any of the IEEE fields of interest. The total number selected in any one year cannot exceed the 0.1% of the total voting membership. IEEE Fellow is the highest grade of membership and is recognized by the technical and scientific community as a prestigious honor and an important career achievement.
- The 2PARMA European Project, coordinated by Cristina Silvano, has been selected in 2013 as a ***"success story"*** by the panel of experts from the Directorate-General for Communications, Networks, Content and Technology (DG-CONNECT) of the European Commission: *"for significant contributions to the state-of-the-art in the field"*. The 2PARMA project has been presented as one of the success stories during the Conference: "Cyber-Physical Systems: Uplifting Europe's innovation capacity", 29-30 Oct. 2013 in Brussels.
- **HiPEAC 2010 Paper Award,** given by the Steering Committee of the HiPEAC Network of Excellence as co-author of the paper: "A Correlation-Based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip " by G. Mariani, G. Palermo, V. Zaccaria, A. Brankovic, J. Jovic, C. Silvano. In Proceedings of **DAC-47** - Design Automation Conference, Anaheim, CA, USA, June 2010, pp. 120-125 url: http://www.hipeac.net/award
- In 2008, the paper titled: "Address Bus Encoding Techniques for System-Level Power Optimization", by L. Benini, G. De Micheli, E. Macii, D. Sciuto, C. Silvano, **DATE-98** [C82] has been recognized as one of **the most influential papers** of the past ten years DATE and then selected to be re-published as a chapter of the volume: **Design, Automation, and Test in Europe - The Most Influential Papers of 10 Years DATE** Lauwereins, Rudy; Madsen, Jan (Eds.), 2008.
- **ACM Recognition of Service Award,** given in Appreciation for Contributions to ACM as General Co-Chair MICRO-41: The 41st Annual IEEE/ACM Int. Symposium on Microarchitecture, Nov. 8-12, 2008.
- **ACM Best Paper Award** given at the 23rd Annual ACM Symposium on Applied Computing (Applications Theme) as co-author of: M. Sykora, G. Agosta e C. Silvano, "Dynamic Configuration of Application Specific Implicit Instructions for Embedded Pipelined Processors", Fortaleza, Brazil, 16-20 March, 2008 [C45].
- **Bull Technical Award 1991**, given by Bull HN Information Systems for my contribution to the project: *"Integrated CAD framework for complex ASIC design"*. The award has been motivated by my contribution to the solution to relevant technical problems demonstrating high professional competences, originality approach and constant personal commitment.

Milano, January 14th, 2019