CV SUMMARY - CRISTINA SILVANO

EDUCATION

1999 **PhD in Information Engineering,** Università degli Studi di Brescia, Italy.
1987 **Master of Science in Electronics Engineering,** Politecnico di Milano, Italy (Final Grade 100/100).

ACADEMIC CAREER

2020 – present **Elected Chair** of the Research Area on Computer Science and Engineering (incl. 96 faculty members) at the Department of Electronics, Information and Bioengineering, Politecnico di Milano.
2022 – 2023 **Promoter** of the new Master of Science Degree in HPC Engineering at Politecnico di Milano (M. Sc. started in AY 2022/23 with 40 pioneering students; in AY 2024/25 reached aroud 100 newly enrolled students).
2022 – present **Member** of the National Technical Committee on Semiconductor Technologies appointed by the Italian Ministry of University and Research (D. M. 455, May 13, 2022).
2019 – 2021 **Vice-Chair** for Computer Science and Engineering, PhD Board in Information Technoloogy, POLIMI.
2018 – present **Full Professor** in Computer Engineering, DEIB, Politecnico di Milano, Italy.
2002 – 2018 **Associate Professor** in Computer Engineering, DEIB, Politecnico di Milano, Italy.
2000 – 2002 **Assistant Professor** in Computer Science, Dept. of Computer Science, Università degli Studi di Milano, Italy.
1999 – 2000 **Post-Doc Researcher** at CEFRIEL / DEIB, Politecnico di Milano, Italy.
1996 – 1998 **Ph.D. Student,** Dept. of Information and Automation Eng., Università degli Studi di Brescia, Italy.

INDUSTRIAL CAREER

1993 – 1994 **Senior Visiting Design Engineer** at IBM Somerset Design Center, Austin (TX - USA).
1992 – 1996 **Senior Design Engineer** in the Bull-IBM Design Team of first worldwide multiprocessor chip set based on IBM PowerPC processor, commercialized in Bull Escala UNIX Servers and IBM RS/6000 Multiprocessor Servers.
1990 **Visiting Design Engineer** at VLSI Technology, in Munich (D) and S. Jose (CA-USA).
1988 – 1989 **Visiting Design Engineer** at Honeywell-Bull R&D Labs, Billerica (MA - USA).
1987 – 1992 **Design Engineer** at Research & Development Labs of Group Bull, Pregnana Milanese, Italy.

RESEARCH INTERESTS

- **Computer Architectures:** Energy-efficient parallel computer architectures, Low-power design for embedded manycores, accelerators for deep neural networks, High Performace Computing techniques for drug discovery applications.
- **Electronic Design Automation:** design space exploration of energy-efficient computer architectures, runtime management for manycores, application and compiler autotuning based on machine learning, co-design techniques.

LEADERSHIP IN RESEARCH PROJECTS (SELECTION)

2022 – present **Leader** of Flagship Project on Accelerators, Spoke on Future HPC & Big Data, **ICSC** Italian National Research Center for HPC, Big Data & Quantum Computing, funded by National Recovery & Resilience Plan, 320M€.
2015 – 2018 **Project Manager** of the IBM/POLIMI Collaborative Innovation Center on Big Data Analytics.
2015 – 2018 **Project Coordinator** (Principal Investigator), EU Project **ANTAREX,** Call H2020-FET-HPC-1-2014, 3M€, Partners: POLIMI, ETH Zurich, Univ. of Porto, INRIA; CINECA, IT4Innovations, Dompé, Sygic.
2010 – 2013 **Project Coordinator** (Principal Investigator), EU Project **2PARMA** Call FP7-ICT-4-2009, 2.7M€, Partners: POLIMI, STMicro, HHI-Fraunhofer Inst., IMEC, Univ. of Athens, RWTH Aachen Univ., Synopsys
2008 – 2010 **Project Coordinator** (Principal Investigator), EU Project **MULTICUBE**, Call FP7-ICT-1-2007, 2.1M€, Partners: POLIMI, DS2, STMicro, IMEC, ESTECO, USI, Univ. Cantabria, Chinese Academy of Sciences.
2003 – 2008 **Principal Investigator** of two 3-year Research Grants funded by STMicroelectronics (60K€ each).

RECENT RESEARCH PROJECTS: EUMASTER4HPC, EXCALATE4COV, AI4DI, LIGATE.

SCIENTIFIC PRODUCTION AND IMPACT

- **Scientific Productivity:** More than **200** publications (**193** entries and **258** co-authors on Scopus):
  - Co-author of more than **40** papers on top-tier journals including IEEE/ACM Transactions and ACM Computing Survey;
  - Co-author of about **120** papers on top-tier conferences including DAC, ICCAD, ASP-DAC, DATE, CODES-ISSS, CASES;
  - Co-editor of **3** scientific books: "Near Threshold Computing", Springer (2015), "Low-Power Networks-on-Chip", Springer (2010), "Multi-objective design space exploration of multiprocessor SoC architectures", Springer (2011);
  - Co-author of **2** scientific books: "Automatic Tuning of Compilers using Machine Learning" Springer (2018), "Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems", Kluwer (2003);
  - Co-inventor of some international patents owned by Group Bull / STMicro Link to patents on Google Scholar
- **Publication Impact: 42** h-index and **5400+** citations according to Google Scholar. Link to Google Scholar profile

AWARDS AND RECOGNITIONS (SELECTION)

2021 **IEEE Certificate of Excellence** for Editorial Service, IEEE Transactions on Computers;
2020 **IEEE/ACM Certificate of Appreciation** *"for an inspiring Keynote Talk at MICRO-53",* Int. Symp. on Microarchitecture;
2019 **ANTAREX Project** recognized as **Success Story** of the European Commission;
2017 **IEEE Fellow** "for contributions to energy-efficient computer architectures";
2013 **2PARMA Project** recognized as **Success Story** of the European Commission;
2010 **HiPEAC 2010 Paper Award** for her paper published at DAC 2010;

2008 **Recipient** co-author of one paper in "The Most Influential Papers of 10 Years DATE";
2008 **ACM Recognition of Service Award** for contributions as General Co-chair MICRO-41;
2008 **ACM Best Paper Award** at ACM Symposium on Applied Computing 2008;
1991 **Group Bull Technical Award** for contributions to an integrated CAD framework for complex ASIC design.

INVITED TALKS AND SEMINARS (SELECTION)

Over **40** invited talks/seminars at international events, among them:
2024 Seminar at NANDA2024 Workshop organized at Imperial College, London;
2024 Panelist at "Future skills needed on HPC", EuroHPC 2024 Summit, Antwerp, Belgium;
2022 Keynote Speaker at SAMOS 2022, Int. Conf. on Embedded Computer Systems;
2020 Keynote Speaker at MICRO 2020, 53rd IEEE/ACM Int. Symposium on Microarchiteture, Virtual Event, October 2020;
2019 Keynote Speaker at High Performance Intelligent Computing Summit, Shenzhen, China;
2017 Keynote Speaker at HeteroPar2017 Workshop, co-located to EuroPar Conference, Santiago de Compostela, Spain;
2016 Seminar at Brain Inspired Computing Group, IBM Research, Austin and Seminar at U. of Texas at Austin, ECE;
2015 Keynote Speaker at the 13th IEEE Int. Conf. EUC 2015 / 18th IEEE Int. Conf.CSE 2015;
2012 Seminar at Intel Labs, Santa Clara, CA, USA;
2010 Seminar at U. of California at Irvine and U. of California at Riverside, Dept. of CSE;
2010 Seminar at Delft Technical University, Computer Engineering Colloquium Series;
2009 Seminar at Princeton University, Dept. of Electrical and Computer Engineering;
2009 Seminar & HP Labs, Palo Alto, CA, USA.

TEACHING EXPERIENCE

Balanced effort in teaching at the Bachelor & Master levels. Current courses held at Politecnico di Milano:
- Advanced Computer Architectures (5 credits), mandatory course offered at the M. Sc. in Computer Engineering & M. Sc. HPC Engineering, POLIMI (Course taught in English), **250+** M.Sc. students per year.
- Computer Architectures & OS (10 credits), B.Sc. in Computer Engineering, POLIMI, (Course taught in Italian), **230+** students.

SERVICES AND MENTORING (SELECTION)

2003 – 2019 **Member** of the Committee on Graduate Admissions in Computer Engineering, POLIMI.
2002 – 2019 **Member** of the Committee on Undergraduate Study Plans and Transfers in Computer Engineering, POLIMI.
2002 – present **Advisor/Co-advisor** of **70+** Master Students in Computer Engineering, POLIMI
2002 – present **Advisor/Co-advisor** of **12** Ph.D. students at Politecnico di Milano, **2** Ph.D. Students at Università della Svizzera Italiana (USI) and **4** Post-doc Students at Politecnico di Milano.
2009 – present **Opponent Member** in **15** Ph.D. Examination Committees at U. of Verona, Politecnico di Torino, Norwegian U. of Science & Tech., RWTH Aachen U., TU Athens, TU Eindhoeven, TU Delft, U. Politecnica de Catalunia, U. of Porto, U. Paris-Saclay, U. of Chalmers.

INTERNATIONAL SERVICES (SELECTION)

Active contributor to the scientific community serving as **Technical Program Committee Member** of several top-tier conferences such as DAC, ICCAD, DATE, NOCS, PACT, HPCA, IPDPS, ISCA, PACT, ASAP and FPL.
2021/2022 **Program Chair** HiPEAC 2021 Conference (virtual evenet), **General Chair,** HiPEAC 2022 Conference, Budapest;
2019 **General Co-Chair,** IEEE/ACM Network-on-Chip Symposium (NOCS), New York, US;
2015, 2016, 2021, 2023, 2024 **Track Chair,** IEEE/ACM Int. Conference on Computer-Aided Design (ICCAD);
2015 – 2017 **Track Chair/Track Co-chair,** IEEE/ACM Design and Test in Europe Conference (DATE);
2012, 2015 **Sub-committee Chair,** IEEE/ACM Design Automation Conference (DAC);
2015 **Program Chair,** 25th Int. Conf. on Field Programmable Logic and Applications, London, UK;
2012 **Program Co-Chair,** 23rd IEEE Int. Conf. on Application-specific Systems, Arch. and Processors (ASAP), Delft, NL;
2009 – 2010 **General/Program Co-Chair,** IEEE Symp. on Application Specific Processors, co-located with DAC, CA;
2008 **General Co-Chair,** 41st IEEE/ACM Int. Symposium on Micro-architecture, Como, IT.

COMMISSIONS OF TRUST (SELECTION)

2024 – present **Member** of the Selection Committee, ACM - IEEE CS Eckert-Mauchly Award;
2024 – present **Associate Editor-in-Chief for Architectures,** Elsevier Journal of Parallel and Distributed Computing;
2022 – 2024 **Member/Chair** of the Selection Committee, IEEE TCCA Young Computer Architect Award;
2021 – 2023 **Evaluator for IEEE Fellow Committee,** IEEE Council on Electronic Design Automation;
2021 – present **Associate Editor,** IEEE Computer Architecture Letters;
2021 – present **Lead Topical Editor,** IEEE Transactions on Computers (TC), formerly **Associate Editor** (2029-2020);
2017 – 2020 **Evaluator for IEEE Fellow Committee,** IEEE Computer Society;
2017 – 2018 **Steering Group Member,** UK Engineering and Physical Sciences Research Council, UK;
2015 – present **Associate Editor,** ACM Transactions on Architecture and Code optimization (TACO);
2008 – 2009 **Member/Chair** of the Review Panel for Computer Science, Academy of Finland, FL;
2007 – 2017 **Expert Reviewer,** INRIA (FR) / Agence Nat. de la Recherche (FR) / Swiss Nat. Science Foundation (CH);
2005 – 2015 **Independent Expert Reviewer,** European Commission for FP6, FP7, FET-Open and Artemis JU frameworks.