CV SUMMARY - CRISTINA SILVANO

EDUCATION

1999 **PhD Degree** in Information Engineering, Università degli Studi di Brescia, Italy.
1987 **Master of Science Degree** in Electrical Engineering, Politecnico di Milano, Italy (Final Grade 100/100).

CAREER

2018 – present **Full Professor** in Computer Engineering, Dept. of Electronics, Information and Bioengineering (DEIB), Politecnico di Milano, Italy
2002 – 2018 **Associate Professor** in Computer Engineering, DEIB, Politecnico di Milano, Italy
2000 – 2002 **Assistant Professor** in Computer Science, Dept. of Computer Science, Univ. degli Studi di Milano, Italy
1999 – 2000 **Post-Doc Researcher** (Assegnista di Ricerca), DEIB, Politecnico di Milano, Italy
1999 **Post-Doc Researcher** at CEFRIEL, Milano, Italy
1996 – 1998 **Ph.D. Student,** Università degli Studi di Brescia, Italy
1987 – 1996 **Design Engineer** (**Senior Design Engineer** since 1993), R&D Labs of Group Bull, Pregnana M., Italy

RESEARCH INTERESTS

Currently **Principal Investigator** of a research group focused on application autotuning and adaptivity for energy-efficient High Performance Computing systems. Main research interests are focused on:

- **Computer Architectures:** energy-efficient computer architectures, embedded architectures, manycore architectures, Networks-on-Chip, technology-aware architecture design, VLIW (Very Long Instruction Word) processor architectures.
- **Electronic Design Automation:** low-power design for embedded systems, design space exploration of energy-efficient computer architectures, runtime management for manycores, compiler autotuning based on machine learning.

LEADERSHIP IN RESEARCH PROJECTS

2015 – 2018 **Project Coordinator** (Principal Investigator), EU Project **ANTAREX** (3M€), Call H2020-FET-HPC-1-2014 Partners: POLIMI, ETH Zurich, Univ. of Porto, INRIA; CINECA, IT4Innovations, Dompé, Sygic.
2010 – 2013 **Project Coordinator** (Principal Investigator), EU Project **2PARMA** (2.7M€), Call FP7-ICT-4-2009 Partners: POLIMI, STMicro, HHI-Fraunhofer Inst., IMEC, Univ. of Athens, RWTH Aachen Univ., Synopsys
2008 – 2010 **Project Coordinator** (Principal Investigator), EU Project **MULTICUBE** (2.1M€), Call FP7-ICT-1-2007 Partners: POLIMI, DS2, STMicro, IMEC, ESTECO, USI, Univ. Cantabria, Chinese Academy of Sciences.
2006 – 2008 **Principal Investigator,** Research Grant funded by STMicroelectronics (60K€)
2003 – 2005 **Principal Investigator,** Research Grant funded by STMicroelectronics (60K€)

ONGOING RESEARCH PROJECTS: ANTAREX4ZIKA, EXSCALATE, EXCALATE4COV, AI4DI.

SCIENTIFIC PRODUCTION AND METRICS

LINK TO MY PUBLICATIONS ON DBLP

- **Scientific Productivity:** More than **200** publications (**181** entries and **220** co-authors on Scopus):
  - Co-author of **38** top-ranked journal papers including **21 IEEE/ACM Transactions** and **1 ACM Computing Survey;**
  - Co-author of more than **100** scientific publications on peer-reviewed conferences including top-level conferences (such as DAC, ICCAD, ASP-DAC, DATE, CODES-ISSS, CASES);
  - Co-editor of **3** scientific books: "Near Threshold Computing", Springer (2015), "Low-Power Networks-on-Chip", Springer (2010), "Multi-objective design space exploration of multiprocessor SoC architectures", Springer (2011);
  - Co-author of **2** scientific books: "Automatic Tuning of Compilers using Machine Learning" Springer (2018), "Power Estimation and Optimization Methodologies for VLIW-based Embedded Systems", Kluwer (2003);
  - Inventor/Co-inventor of **11** patent applications with Group Bull and STMicro (**7** out of **11** already granted).
- **Publication Impact: 35** h-index and **4000+** citations according to Google Scholar. **Link to my page on Google Scholar**

AWARDS AND RECOGNITIONS (SELECTION)

2019 **ANTAREX Project** recognized as **Success Story** of the DG-CONNECT of the European Commission.
2017 **IEEE Fellow** "for contributions to energy-efficient computer architectures"
2013 **2PARMA Project** recognized as **Success Story** of the DG-CONNECT of the European Commission.
2010 **HiPEAC 2010 Paper Award** as co-author of a paper published at DAC 2010.
2008 **Recipient** co-author of one of "The Most Influential Papers of 10 Years DATE".
2008 **ACM Recognition of Service Award** for contributions as General Co-chair MICRO-41
2008 **ACM Best Paper Award** at ACM Symposium on Applied Computing 2008.
1991 **Bull Technical Award** "for contributions to an integrated CAD framework for complex ASIC design"

INVITED TALKS AND SEMINARS (SELECTION)

Over **25** invited talks/seminars at international venues. Among them:

2019 Keynote Speaker at High Performance Intelligent Computing Summit, Shenzhen, China
2017 Keynote Speaker at HeteroPar2017 Workshop, co-located to EuroPar Conference, Santiago, Spain
2016 Seminar at Brain Inspired Computing Group, IBM Research, Austin
2016 Seminar at the University of Texas at Austin, ECE, Computer Architecture Seminar Series
2015 Keynote Speaker at the 13th IEEE Int. Conf. EUC 2015 / 18th IEEE Int. Conf.CSE 2015
2012 Seminar at Intel Labs, Santa Clara, CA, USA

2010 Seminar at University of California Riverside, Dept. of Computer Science & Engineering
2010 Seminar at University of California Irvine, Dept. of Computer Science & Engineering
2010 Seminar at Delft Technical University, Computer Engineering Colloquium Series
2009 Seminar at Princeton University, Dept. of EE, Computer Engineering Seminar & HP Labs, Palo Alto, CA, USA

TEACHING EXPERIENCE

Balanced effort in teaching at **B.Sc.** & **M.Sc. levels**. Current courses held at Politecnico di Milano in 2019/2020:

- Advanced Computer Architectures (5 credits), M. Sc. in Computer Engineering, POLIMI (Course in English), **250+** students
- Computer Architectures & Operating Systems (10 credits), B.Sc. in Computer Engineering, POLIMI, (Course in Italian), **200+** students
- Computer Architectures for Deep Neural Networks (5 credits), PhD. Program in Information Technology, POLIMI.

INSTITUTIONAL RESPONSIBILITIES AT POLIMI (SELECTION)

2020 – present **Chair** of the Research Area on Computer Science and Engineering at DEIB, Politecnico di Milano.
2019 – present **Vice-Chair** of the PhD Program on Computer Science and Engineering, Politecnico di Milano.
2015 – 2018 **Project Manager** of the IBM/POLIMI Collaborative Innovation Center on Big Data Analytics
2003 – 2019 **Member** of the Committee on Graduate Admissions in Computer Engineering, Politecnico di Milano, Como Campus (2003-2017), Leonardo Campus (2015-2019).
2002 – 2019 **Member** of the Committee on Undergraduate Study Plans and Transfers in Computer Engineering, Politecnico di Milano, Como Campus.
2002 – present **Advisor/Co-advisor** of **60+** Master Students in Computer Engineering, School of Industrial and Information Engineering, Politecnico di Milano

SUPERVISION OF DOCTORAL AND POSTDOCTORAL STUDENTS

2002 – present **Advisor/Co-advisor** of **11** Doctoral Students at Politecnico di Milano, **2** Doctoral Students at Università della Svizzera Italiana (USI) and **2** Postdoctoral Students at Politecnico di Milano.
2009 – present **Opponent Member** of **9** Doctoral Examination Committees at TU Athens, Univ. of Verona, Politecnico di Torino, Norwegian Univ. of Science & Tech., RWTH Aachen Univ., TU Eindhoven, TU Delft, Univ. Politecnica de Catalunia, Univ. of Porto.

ORGANIZATION OF SCIENTIFIC MEETINGS (SELECTION)

Active contributor to the scientific community serving regularly in the Technical Program Committee of several top-level conferences such as DAC, ICCAD, DATE, NOCS, PACT, MICRO, IPDPS, PACT, ASAP and FPL. Among them:

2015 – 2017 **Track Chair/Track Co-chair,** IEEE/ACM Design and Test in Europe Conference (DATE)
2015 – 2016 **Track Chair,** IEEE/ACM Int. Conference on Computer-Aided Design (ICCAD)
2012, 2015 **Sub-committee Chair,** IEEE/ACM Design Automation Conference (DAC)
2019 **General Co-Chair,** IEEE/ACM Network-on-Chip Symposium (NOCS), New York, US
2015 **Program Chair,** 25th Int. Conf. on Field Programmable Logic and Applications, London, UK
2012 **Program Co-Chair,** 23rd IEEE Int. Conf. on Application-specific Systems, Arch. and Processors (ASAP), Delft, NL
2010 **Program Co-Chair,** IEEE Symposium on Application Specific Processors, co-located with DAC, Anaheim, CA
2009 **General Co-Chair,** IEEE Symposium on Application Specific Processors, co-located with DAC, San Francisco, CA
2008 **General Co-Chair,** 41st IEEE/ACM Int. Symposium on Micro-architecture, Como, IT

COMMISSIONS OF TRUST (SELECTION)

2019 – present **Associate Editor,** IEEE Transactions on Computers (TC)
2017 – present **Steering Group Member,** UK Engineering and Physical Sciences Research Council, UK
2017 – present **Expert Reviewer,** FWO (Research Foudation Flanders), BE
2016 – present **Expert Reviewer,** Swiss National Science Foundation, CH
2015 – present **Associate Editor,** ACM Transactions on Architecture and Code optimization (TACO)
2013 – 2015 **Associate Editor,** MICPRO Journal, Embedded HW Design (Microprocessor and Microsystems), Elsevier
2013 – 2015 **Independent Expert Reviewer,** European Commission, ARTEMIS JU Project
2010 **Expert Reviewer,** Programme Blanc Int., Agence Nationale de la Recherche, FR
2009 – 2013 **Independent Expert Reviewer,** European Commission, FET-Open Programme
2008 – 2009 **Member/Chair** of the Review Panel for Computer Science, Academy of Finland, FL
2007 **Primary Evaluator,** INRIA (French National Institute for Computer Science), FR
2005 – 2014 **Independent Expert Reviewer,** EU Commission, FP6 and FP7 Projects and Network of Excellence HiPEAC

INDUSTRIAL EXPERIENCE

1993 – 1994 **Visiting Engineer** at IBM Somerset Design Center, Austin (TX - USA).
1992 – 1996 **Member of Bull-IBM Design Team** of the first worldwide multiprocessor system based on IBM PowerPC, commercialized as Bull Escala UNIX Servers and as IBM RS/6000 Multiprocessor Servers.
1990 **Visiting Engineer** at VLSI Technology, in Munich (D) and in S. Jose (CA-USA)
1988 – 1989 **Visiting Engineer** at Honeywell-Bull R&D Labs, Billerica (MA - USA)
1987 – 1996 **Design Engineer** (since 1993 **Senior Design Engineer**) at R&D Labs of Group Bull in Italy.