Curriculum Vitae – Daniele Ielmini

Present Position

Full Professor
Dipartimento di Elettronica, Informazione e Bioingegneria
Politecnico di Milano
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Previous positions

2010 – 2016	Associate Professor, Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano
2010	Visiting Professor, University of Illinois at Urbana-Champaign (UIUC)
2002 – 2010	Assistant Professor, Dipartimento di Elettronica e Informazione, Politecnico di Milano
2006	Visiting Professor, Intel Corporation and Center for Integrated Systems (CIS) – Stanford University
2000 – 2002	Research Assistant, Dipartimento di Elettronica e Informazione, Politecnico di Milano

Education

1997 – 2000	Ph.D., Nuclear Engineering, Politecnico di Milano
1989 – 1995	Laurea, Nuclear Engineering, Politecnico di Milano

Awards and Recognition

2019	Fellow, IEEE
2015	Highly Cited Researcher, Thomson Reuters
2014	ERC Consolidator Grant
2013	Intel Outstanding Researcher Award for Devices
2009	Senior Member, IEEE

Best Paper Awards

2015	IEEE EDS Paul Rappaport Award for the paper “Noise-Induced Resistance Broadening in Resistive Switching Memory—Part I: Intrinsic Cell Behavior and Part II: Array Statistics,” by S. Ambrogio, S. Balatti, V. McCaffrey, D. C. Wang, and D. Ielmini, as the best paper in the IEEE Trans. Electron Devices over 630 papers that were published in 2015.
2014	Best Poster Award for the paper “Voltage-Dependent Random Telegraph Noise (RTN) in HfO_x Resistive RAM,” by S. Balatti, S. Ambrogio, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini, presented by S. Balatti at the International Reliability Physics Symposium (IRPS) 2014
2013	Best Paper Award for the paper “Resistive Switching in Metal Oxides: From Physical Modeling to Device Scaling,” by D. Ielmini, S. Balatti, and S. Ambrogio, presented by D. Ielmini at 224th ECS, Oct 27-Nov 1, 2013.
2011	Best Student Paper Award for the paper “Filament diffusion model for simulating reset and retention processes in RRAM,” by S. Larentis, C. Cagli, F. Nardi and D. Ielmini, presented by S. Larentis at the Insulating Films on Semiconductors (INFOS) 2011
2007	Impressive Award for Best Presentation at the European Phase Change and Ovonic Science Symposium, E/PCOS 2007

Conference Organizations

2017 – 2018	International Electron Device Meeting (IEDM), Subcommittee Member for Memory Technology
2018 – 2019	NANOARCH, Member of the Program Committee
2017	Design, Automation, and Test in Europe (DATE), Member of the Technical Committee
2017	ISCAS, organized the Special Session ‘Computing with memory devices’
2016 – 2019	ISCAS, Member of the NanoGiga Technical Committee
2015 – 2019	European Phase Change and Ovonic Science Symposium (E/PCOS), Member of the Program Committee
2015	European Material Research Symposium (EMRS), Member of the Scientific Committee
2014	CAS-FEST 2014, Special Session Organizer
2014 – 2018	CIMTEC, Forum of Novel Materials, Member of the Technical Committee
2013	PACRIM10, Member and Contact of the Technical Committee
2013 – 2019	Chinese Semiconductor Technology International Conference (CSTIC), Member of the Technical Committee
2012	NonVolatile Memory Technology Symposium (NVMTS), Session Chair

2012	European Material Research Symposium (EMRS), Member of the Scientific Committee
2011 – 2017	Insulating Films on Semiconductors (INFOS), Member of the Technical Committee
2008 – 2010	Semiconductor Interface Specialist Conference (SISC), Member of the Technical Committee
2008 – 2009	International Electron Device Meeting (IEDM), Subcommittee Member for Memory Technology
2007	International Reliability Physics Symposium (IRPS), Workshop organizer and moderator for Non volatile memory
2006 – 2008	International Reliability Physics Symposium (IRPS), Subcommittee Member for Dielectrics and Memory

Instructor

2019	Tutorial on “Emerging nonvolatile memory technologies,” IEEE Electron Device Technology and Manufacturing (EDTM), Singapore, Mar. 12-15, 2019.
2018	Tutorial on “Embedded memory technologies,” IEEE International Conference on IC Design and Technology (ICICDT), Otranto, Italy, June 4-6, 2018.
2017	Tutorial on “Resistive memory: switching mechanisms, models, and applications in computing,” 2017 SIE Meeting, Palermo, Italy, June 19-23, 2017.
2017	Tutorial on “Memristive devices, circuits, systems and applications,” 2017 IEEE-ISCAS, Baltimore, MD, USA, May 28-31, 2017.
2017	Tutorial on “Physics of emerging devices,” 2017 International Memory Workshop (IEEE-IMW, 2017), Monterey, CA, USA, May 14-17, 2017.
2017	Lecture on “High density ReRAM and PCRAM,” 2017 1st Electron Devices Technology and Manufacturing Conference (IEEE-EDTM, 2017)
2016	Tutorial on Memristive devices and neuromorphic networks, Material Research Society Fall Meeting (MRS 2016)
2016	Tutorial on Memristive Theory and Modeling, Second Training Course on Memristors - Devices, Models, Circuits, Systems and Applications (MemoCIS), Alghero, May 7-9 (2016)
2015	Lecture on “Emerging memory technologies: ReRAM and PCM”, in 2015 IEDM short course on “Memory Technologies for Future Systems”, Washington DC, USA, Dec. 7-9 (2015)
2015	Tutorial on Memristive Switching Mechanisms, First Training Course on Memristors - Devices, Models, Circuits, Systems and Applications (MemoCIS), Alghero, May 9-12 (2015)
2013	Tutorial on Resistive switching memory mechanisms, International Memory Workshop (IEEE-IMW 2013)
2012	Tutorial on Resistive switching memory modeling, Material Research Society Spring Meeting (MRS 2012)
2011	Tutorial on Phase change memory modeling, Material Research Society Spring Meeting (MRS 2011)
2011	Tutorial on Resistance switching and memristive computing, Nano Giga Challenges (NGC 2011)
2010	Tutorial on Phase change memories, Material Research Society Spring Meeting (MRS 2010)
2010	Tutorial on Memory Reliability, European Symposium on Reliability and Failure (ESREF 2010)
2008	Tutorial on Non-Volatile Memories, International Reliability Physics Symposium (IRPS 2008)
2007	Tutorial on Memory Reliability, International Reliability Physics Symposium (IRPS 2007)
2005	Tutorial on Memory Reliability, International Reliability Physics Symposium (IRPS 2005)

Teaching

2002 – 2019	Solid State Electronics, Undergraduate Student Course, EE, Politecnico di Milano (http://home.deib.polimi.it/ielmini/ess.htm)
2006 – 2015	Nonvolatile memories, PhD Course, EE, Politecnico di Milano (http://home.deib.polimi.it/ielmini/nvm.htm)
2015 – 2019	Optoelectronics, Undergraduate Student Course, EE, Politecnico di Milano (http://home.deib.polimi.it/ielmini/oe.htm)
2015 – 2019	New materials and devices for post-Si computing, PhD Course, EE, Politecnico di Milano (http://home.deib.polimi.it/ielmini/psc.htm)
2000 – 2008	Fundamental of Electronics, Undergraduate Student Course, EE, Politecnico di Milano
2008	Nonvolatile Resistive Memories, Graduate Students Course, Master in Technologies for Micro-Nano Electronics, Università degli Studi di Roma ‘La Sapienza’

Editorial activities

2017	J. Electroceramics (Springer), Guest Editor for a Special Issue on ‘Resistive Switching: Oxide Materials, Mechanisms, Devices and Operations’
2017 – 2019	Semiconductor Science and Technology (IOP), Associate Editor
2015 – 2019	IEEE Trans. Nanotechnology, Associate Editor

Journal Reviewer

Nature, Nature Nanotechnology, Nature Communications, Nature Materials, Nature Electronics, Science Advances, Scientific Reports, Advanced Materials, Advanced Functional Materials, Nano Letters, ACS Nano, Nanoscale, Applied Physics Letters, Journal of Applied Physics, IEEE Transactions on Electron Devices, IEEE Electron Device Letters, AIP Advances, Nanotechnology, and others.

Professional Memberships

Institute of Electrical and Electronics Engineers (IEEE, Fellow)

General Research Interests

Research interests are focused on CMOS and post-CMOS devices and circuits, particularly regarding the characterization and modeling of memory devices and their scaling challenges. My research activity has been devoted to the following topics:

- CMOS front-end reliability (dielectric trapping and leakage effects, hot carrier effects, NBTI)
- Modeling and characterization of CMOS-based non-volatile memories (Flash, nanocrystal, charge-trap memories)
- Modeling and characterization of emerging nonvolatile memories (phase change memory – PCM, resistive switching memory – RRAM, conductive bridge memory – CBRAM, spin-torque transfer magnetic memory – STTRAM)
- Development of nanowire-based resistive-switching nanodevices for ultrascaled nonvolatile memories and logic
- Neuromorphic circuits integrating CMOS and resistive switches for pattern learning and recognition

Ph.D./Postdoc Student Supervisor

Christian Monzio Compagnoni (Ph.D., 2005, now Associate Professor at Politecnico di Milano, Italy)
Deepak Sharma (Post doc, 2006 – 2008, now Professor at SCRIET, Meerut, India)
Davide Mantegazza (MS 2004, Ph.D. 2008, now with Intel)
Ugo Russo (MS 2005, Ph.D. 2009, now with Micron)
Simone Lavizzari (MS 2006, Ph.D. 2010, now with Prophesee)
Carlo Cagli (MS 2007, Ph.D. 2011, now with CEA-LETI)
Davide Fugazza (Ph.D. 2011, now with Intel)
Mattia Boniardi (Ph.D. 2011, now with Micron)
Federico Nardi (MS 2008, Ph.D. 2012, now with Western Digital)
Maurizio Rizzi (MS 2011, Ph.D. 2014, now with Micron)
Seol Choi (Post doc, 2011-2012, now with Samsung)
Nicola Ciocchini (MS 2011, Ph.D. 2015, now with Intel)
Simone Balatti (MS 2011, Ph.D. 2015, now with Intermolecular)
Stefano Ambrogio (MS 2012, Ph.D. 2016, now with IBM)
ZhongQiang Wang (Post doc, 2014-2016, now Associate Professor at Northeast Normal University, Changchun, China)
Mario Laudato (MS 2014, Ph.D. 2018, now with Intermolecular)
Valerio Milo (MS 2015, Ph.D. in 2019, now postdoc fellow at Politecnico di Milano, Italy)
Alessandro Bricalli (MS 2015, Ph.D. in 2019, now with Weebit Nano)
Elia Ambrosi (MS 2016, Ph.D. expected in 2020)
Roberto Carboni (MS 2016, Ph.D. expected in 2020)
Giacomo Pedretti (MS 2016, Ph.D. expected in 2020)
Nicola Polino (MS 2016, Ph.D. expected in 2020)
Zhong Sun (Post doc, 2017-2019)
Wang Wei (Post doc, 2017-2019)
Stefano Bianchi (MS 2017, Ph.D. expected in 2021)
Irene Munoz (Ph.D. expected in 2021)
Octavian Melnic (Ph.D. expected in 2021)
Erika Covi (Post doc, 2018-2020)

List of Publications

Books

[1] Resistive switching – from fundamental redox-processes to device applications (Wiley-VCH, 2016), D. Ielmini and R. Waser Eds. (2016). ISBN 978-3-527-33417-9

Book Chapters

[2] D. Ielmini, "Phase change memory device modeling," in Phase Change Materials – Science and Applications, Springer, S. Raoux and M. Wuttig Eds., 299-330 (2009). ISBN 978-0-387-84873-0.
[3] C. Monzio Compagnoni, R. Gusmeroli, A. S. Spinelli, D. Ielmini, A. L. Lacaita and A. Visconti, "Present status and scaling challenges for the NOR Flash memory technology," in Solid State Electronics Research Advances, Nova Science Publishers, Inc., New York, Sergo Kobadze ed., 101-134 (2009). ISBN 978-1-60021-851-4.
[4] C. Cagli and D. Ielmini, "Resistive-Switching Memory Devices Based on Metal Oxides: Modeling of Unipolar Switching, Reliability, and Scaling," in Nonvolatile Memories: Materials, Devices and Applications, edited by Tseung-Yuen Tseng and Simon M. Sze, Volume 2, 225-248 (American Scientific Publishers, 2012). ISBN 1-58883-251-1
[5] D. Ielmini, "Phase Change Memory Physics-Based Modeling: Electrical Characteristics, Scaling, and Reliability," in Nonvolatile Memories: Materials, Devices and Applications, edited by Tseung-Yuen Tseng and Simon M. Sze, Volume 2, 83-109 (American Scientific Publishers, 2012). ISBN 1-58883-251-1
[6] D. Ielmini, "Resistive switching models by ion migration in metal oxides," in Nanoscale Applications for Information and Energy Systems, Series: Nanostructure Science and Technology, Anatoli Korkin and David J. Lockwood (Eds.), XII, 346, 169-202 (Springer, 2013). ISBN 978-1-4614-5015-3. DOI: 10.1007/978-1-4614-5016-0_6
[7] D. Ielmini, "Resistive switching memories," in Wiley Encyclopedia Electrical and Electronic Engineering (EEEE), J. Webster (ed.), 1-32 (2014 John Wiley & Sons, Inc.). DOI: 10.1002/047134608X.W8222. ISBN: 0-471-13946-7.
[8] R. Waser, D. Ielmini, H. Akinaga, H. Shima, H.-S. Philip Wong, J. J. Yang, and S. Yu, "Introduction to Nanoionic Elements for Information Technology," in Resistive switching – from fundamental redox-processes to device applications, (Wiley-VCH, 2016), D. Ielmini and R. Waser Eds. (2016). ISBN 978-3-527-33417-9
[9] D. Ielmini, and S. Menzel, "Universal Switching Behavior," in Resistive switching – from fundamental redox-processes to device applications, (Wiley-VCH, 2016), D. Ielmini and R. Waser Eds. (2016). ISBN 978-3-527-33417-9
[10] D. Ielmini, "Electrical Transport in crystalline and amorphous chalcogenide," in Phase Change Memory: Device Physics, Reliability and Applications, (Springer International Publishing AG 2018), A. Redaelli Ed. 11-39 (2018). ISBN: 978-3-319-69052-0, DOI: 10.1007/978-3-319-69053-7
[11] D. Ielmini and V. Milo, "Brain-inspired memristive neural networks for unsupervised learning," in Handbook of Memristor Networks, G. Sirakoulis and L. Chua eds. (Springer, 2018).
[12] D. Ielmini and S. Ambrogio, "Neuromorphic computing with resistive switching memory devices," in Advances in Non-volatile Memory and Storage Technology, 2nd Edition, B. Magyari-Kope and Y. Nishi eds. (Elsevier, 2018).

Invited Papers in Journals and Conference Proceedings

[13] A. Pirovano, A. Redaelli, F. Pellizzer, F. Ottogalli, M. Tosi, D. Ielmini, A. L. Lacaita and R. Bez, "Reliability study of phase-change non-volatile memories," IEEE Trans. on Device and Material Reliability 4, 422-427 (2004).
[14] D. Ielmini, A. S. Spinelli and A. L. Lacaita, "Recent developments on Flash memory reliability," Proc. INFOS 2005, published on special issue of Microelectron. Eng. 80C, 321-328 (2005).
[15] C. Monzio Compagnoni, R. Gusmeroli, D. Ielmini, A. S. Spinelli, A. L. Lacaita, "Silicon nanocrystal memories: a status update," Journal of Nanoscience and Nanotechnology 7, 193-205 (2007).
[16] D. Ielmini and A. L. Lacaita, "Physical modeling of conduction and switching mechanisms in phase change memory cells," European Phase Change and Ovonics Science Symposium, E*PCOS (2007).
[17] A. L. Lacaita and D. Ielmini, "Status and challenges of phase change memory modeling," European Solid-State Device Research Conference, ESSDERC, 214-221 (2007).
[18] A. L. Lacaita and D. Ielmini, "Reliability issues and scaling projections for phase change non volatile memories," IEDM Tech. Dig.,157-160 (2007).
[19] A. L. Lacaita, U. Russo and D. Ielmini, "Recent advances on the modeling of phase change materials and devices," Mater. Res. Soc. Symp. Proc. 1072-G06-05 (2008).
[20] D. Ielmini, "Modeling of switching phenomena in phase-change memory (PCM) devices," Proc. European Phase-Change and Ovonic Symposium (E*PCOS), 99-108 (2008).
[21] D. Ielmini, "Reliability issues and modeling of Flash and post-Flash memory," Insulating Films on Semiconductors – INFOS, Cambridge, UK (June 2009), also appearing in Microelectron. Eng. 86, 1870-1875 (2009).
[22] D. Ielmini, "Reliability and scaling challenges of phase-change memories from a physical-modeling perspective," 4th International Symposium on Next-generation Non-volatile Memory Technology for Terabit Memory, 131-132 (2009).
[23] D. Ielmini, "Overview of modeling approaches for scaled non-volatile memories," Proc. International Conference on Simulation of Semiconductor Processes and Devices, SISPAD, 9-16 (2009). ISBN 978-1-4244-3947-8.
[24] A. L. Lacaita and D. Ielmini, "Bridging carrier transport and amorphous dynamics in phase change materials," Proceedings of the 2009 European Phase-Change and Ovonic Symposium (E*PCOS), 165-173 (2009).
[25] D. Ielmini, "Modeling of resistance switching and reliability in non-volatile PCM and RRAM," Proc. International Symposium on Integrated Ferroelectrics and Functionalities, ISIF2 108 (2009).
[26] S. Raoux, W. Welnic and D. Ielmini, "Phase change materials and their application to non-volatile memories," Chem. Rev. 110, 240-267 (2010).

[27] D. Ielmini, “Understanding phase change memory reliability and scaling by physical models of the amorphous chalcogenide phase,” Mater. Res. Soc. Symp. Proc. 1251-H05-01 (2010).
[28] D. Ielmini, “Scaling effects of programming and reliability in phase change memory,” ISIF 302-303 (2010).
[29] D. Ielmini, “Size-dependent switching and reliability of NiO RRAMs,” ECS Trans. 33, 3, 323-331 (2010).
[30] D. Ielmini, “Unified physical model of reliability mechanisms and scaling perspective of phase change memory,” Current Applied Phys. 11, e85-e91 (2011).
[31] D. Ielmini, “Universal set/reset characteristics of metal-oxide resistance switching memories,” ECS Trans. 35, 4, 581-596 (2011).
[32] D. Ielmini, D. Fugazza and M. Boniardi, “Energy landscape models for conduction and drift in PCM,” Mater. Res. Soc. Symp. Proc. Vol. 1338 (2011).
[33] D. Ielmini, R. Bruchhaus and R. Waser, “Thermochemical resistive switching: Materials, mechanisms and scaling projections,” Phase Transition 84, 7, 570–602 (2011). DOI:10.1080/01411594.2011.561478
[34] D. Ielmini and D. Fugazza, “Size-dependent random-telegraph noise in phase-change memory (PCM) devices,” EPCOS (2011).
[35] D. Ielmini and A. L. Lacaita, “Phase change materials in non-volatile storage,” Materials Today 14, 600-607 (2011).
[36] D. Ielmini and A. L. Lacaita, “Electrical properties and microscopic structure of amorphous chalcogenides,” Nonvolatile Memory Technology Symposium (2011).
[37] D. Ielmini, “Filamentary-switching model in RRAM for time, energy and scaling projections,” IEDM Tech. Dig. 409-412 (2011).
[38] D. Ielmini, “Phase change memory modeling: From chalcogenide physics to device scaling,” ECS Transactions – CSTIC 2012, Vol. 44, 1227-1234 (2012).
[39] S. Raoux, D. Ielmini, M. Wuttig and I. V. Karpov, “Phase change materials,” MRS Bull. 37, 118-123 (2012).
[40] D. Ielmini, S. Larentis, S. Balatti, F. Nardi and D. Gilmer, “Ion migration model for resistive switching in transition metal oxides,” Nanosession Kick-off Talk, Nature Conference, Technical Digest of Frontiers in Electronic Materials, J. Heber, D. Schlom, Y. Tokura, R. Waser and M. Wuttig, (Eds.), Wiley-VCH, 219-220 (2012). ISBN 978-3-527-41191-7
[41] D. Ielmini, “Switching models for bipolar RRAM devices,” Workshop on Dielectrics in Microelectronics (WoDiM), Dresden, Germany, June 2012.
[42] D. Ielmini, S. Balatti and S. Larentis, “A Physics-based Model of Resistive Switching in Metal Oxides,” International Conference on Solid State Devices and Materials (SSDM), Kyoto, Japan, 25-27 Sept. 2012.
[43] D. Ielmini, “Physical modeling of voltage-driven resistive switching in oxide RRAM,” IEEE International Integrated Reliability Workshop (IIRW) Final Report 9-15 (2012). DOI:10.1109/IIRW.2012.6468905
[44] D. Ielmini, “Modeling of ion-based resistive switching in metal oxides,” NVMTS, Singapore 31 Oct.-2 Nov. 2012.
[45] D. Ielmini, “Electron and ion transport models in metal oxide RRAM,” APS Spring Meeting (2013).
[46] D. Ielmini, “Resistive switching in high-k metal oxides: modeling and scaling,” Mater. Res. Soc. Symp. Proc. (2013).
[47] D. Ielmini, “Resistive switching nanodevices: Models, scaling and applications,” China NANO, Sept. 4-6, 2013.
[48] N. Ciocchini, M. Cassinerio and D. Ielmini, “Crystallization phenomena in phase change memories: non-Arrhenius kinetics, modeling and novel applications,” Proc. European Phase-Change and Ovonic Symposium (E*PCOS) (2013).
[49] A. Behnam, F. Xiong, K. L. Grosse, A. Cappelli, S. Hong, N. Wang, M.-H. Bae, Y. Dai, A.D. Liao, E.A. Carrion, D. Ielmini, E. Piccinini, C. Jacoboni, W. P. King, and E. Pop, “Sub-10 nm Scaling of Phase-Change Memory: Thermoelectric Physics, Carbon Nanotube and Graphene Electrodes,” Proc. European Phase-Change and Ovonic Symposium (E*PCOS) (2013).
[50] D. Ielmini, S. Ambrogio and S. Balatti, “Resistive switching in metal oxides: from physical modeling to device scaling,” in ECS Transactions 58, 165-173 (2013). DOI: 10.1149/05807.0165ecst
[51] S. Ambrogio, S. Balatti, A. Cubeta, D. Ielmini, “Statistical Modeling of Program and Read Variability in Resistive Switching Devices,” IEEE International Symposium on Circuits and Systems (ISCAS), 2029 (2014). DOI: 10.1109/ISCAS.2014.6865563
[52] D. Ielmini, ‘Scaling of resistive switching memories,’ SSDM, Tsukuba, Ibaraki, Japan, September 8-11, 2014.
[53] D. Ielmini, S. Balatti and S. Ambrogio, “Stress-induced asymmetric switching and filament instability in electrochemical memories,” ECS Trans. 64, 169-175 (2014). DOI: 10.1149/06408.0169ecst
[54] D. Ielmini, S. Balatti and S. Ambrogio “Scaling of oxide-based resistive switching devices,” Proc. NVMTS, Jeju Island, Korea, October 25-27, 2014. DOI: 10.1109/NVMTS.2014.7060839
[55] D. Ielmini, “Novel applications of phase change materials: from memory to computing,” E/PCOS15, Amsterdam, NL, Sept. 6-8, 2015.
[56] D. Ielmini, “Logic and neuromorphic computing with resistive switches,” Advances in ReRAM: Materials and Interfaces, Hania, Greece, Oct. 11-16, 2015.
[57] D. Ielmini, “Resistive Switching Memories based on Metal Oxides: Mechanisms, Reliability and Scaling,” Semicond. Sci. Technol. 31, 063002 (2016). DOI: 10.1088/0268-1242/31/6/063002
[58] D. Ielmini, S. Ambrogio, V. Milo, S. Balatti, and Z.-Q. Wang, “Neuromorphic computing with hybrid memristive/CMOS synapses for real-time learning,” 2016 IEEE International Symposium Circuits and Systems (ISCAS), Montreal, Canada, May 22-25, 2016. DOI: 10.1109/ISCAS.2016.7527508
[59] N. Ciocchini, M. Laudato, M. Boniardi, E. Varesi, P. Fantini, A. L. Lacaita and D. Ielmini, “Bipolar switching operation in phase change memory devices for high temperature retention,” E/PCOS16, Sept. 4-6, 2016, Cambridge, UK.
[60] D. Ielmini, “Physical Models of Program and Read Fluctuations in Metal Oxide Resistive RAM,” ECS Trans. 75, 4, 19-26 (2016). DOI: 10.1149/07505.0019ecst
[61] M. Laudato, G. Pedretti and D. Ielmini, “Brain-inspired neuromorphic computing with phase change memory (PCM) synapses,” E/PCOS (2017).
[62] D. Ielmini and V. Milo, “Physics-based modeling approaches of resistive switching devices for memory and in-memory computing applications,” J. Computation. Electron. 16(4), 1121-1143 (2017). DOI: 10.1007/s10825-017-1101-9
[63] V. Milo, D. Ielmini, and E. Chicca, “Attractor networks and associative memories with STDP learning in RRAM synapses,” IEDM Tech. Dig. 263-266 (2017). DOI: 10.1109/IEDM.2017.8268369
[64] D. Ielmini, “Brain-inspired computing with resistive switching memory (RRAM): Devices, synapses and neural networks,” Microelectron. Eng. 190, 44-53 (2018). doi:10.1016/j.mee.2018.01.009

[65] V. Milo, G. Pedretti, M. Laudato, A. Bricalli, E. Ambrosi, S. Bianchi, E. Chicca, and D. Ielmini, “Resistive switching synapses for unsupervised learning in feed-forward and recurrent neural networks,” 2018 IEEE International Symposium Circuits and Systems (ISCAS), Firenze, Italy, May 4-7, 2018.
[66] A. Mehonic, A. L. Shluger, D. Gao, I. Valov, E. Miranda, D. Ielmini, A. Bricalli, E. Ambrosi, C. Li, J. J. Yang, Q. Xia, and A. J. Kenyon, “Silicon Oxide (SiO_x) – A Promising Material for Resistance Switching?” Adv. Mater. (2018). Doi: 10.1002/adma.201801187
[67] D. Ielmini and H.-S. P. Wong, “In-memory computing with resistive switching devices,” Nature Electronics 1, 333-343 (2018). doi: 10.1038/s41928-018-0092-2
[68] D. Ielmini, “Calcolo neuromorfico: circuiti elettronici che imitano la mente umana,” Mondo Digitale 79 Dicembre (2018).

International Refereed Journals

[69] G. Ghislotti, D. Ielmini, E. Riedo, M. Martinelli and M. Dellagiovanna, “Picosecond time-resolved luminescence studies of recombination processes in CdTe,” Solid State Commun. 111, 211-216 (1999).
[70] G. Ghislotti, E. Riedo, D. Ielmini and M. Martinelli, “Intersubband relaxation time for $In_xGa_{1-x}As$/AlAs quantum wells with large transition energy,” Appl. Phys. Lett. 75, 3626-3628 (1999).
[71] A. S. Spinelli, A. L. Lacaita, M. Rigamonti, D. Ielmini and G. Ghidini, “Separation of electron and hole traps by transient current analysis,” Microelectron. Eng. 48, 151-154 (1999).
[72] D. Ielmini, A. S. Spinelli and A. L. Lacaita, “Experimental evidence for recombination-assisted leakage in thin oxides,” Appl. Phys. Lett. 76, 1719-1721 (2000).
[73] D. Ielmini, A. S. Spinelli, A. L. Lacaita, A. Martinelli and G. Ghidini, “A recombination model for transient and stationary stress-induced leakage current,” Microelectron. Reliab. 40, 703-706 (2000).
[74] D. Ielmini, A. S. Spinelli, M. A. Rigamonti and A. L. Lacaita, “Modeling of SILC based on electron and hole tunneling - Part I: Transient effects,” IEEE Trans. Electron Devices 47, 1258-1265 (2000).
[75] D. Ielmini, A. S. Spinelli, M. A. Rigamonti and A. L. Lacaita, “Modeling of SILC based on electron and hole tunneling - Part II: Steady-state,” IEEE Trans. Electron Devices 47, 1266-1272 (2000).
[76] D. Ielmini, A. S. Spinelli, M. Beretta and A. L. Lacaita, “Different types of defect in the silicon dioxides characterized by their transient behavior,” J. Appl. Phys. 89, 4189-4191 (2001).
[77] D. Ielmini, A. S. Spinelli, A. L. Lacaita, D. J. DiMaria and G. Ghidini “A Detailed investigation of the quantum yield experiment,” IEEE Trans. Electron Devices 48, 1696-1702 (2001).
[78] D. Ielmini, A. S. Spinelli, A. L. Lacaita, A. Martinelli and G. Ghidini, “A recombination- and trap-assisted tunneling model for stress-induced leakage current,” Solid State Electronics 45, 1361-1369 (2001).
[79] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “A new two-trap tunneling model for the anomalous SILC in flash memories,” Microelectron. Eng. 59, 189-195 (2001).
[80] D. Ielmini, A. S. Spinelli, A. L. Lacaita and A. Modelli, “Equivalent cell approach for extraction of the SILC distribution in Flash EEPROM cells,” IEEE Electron Device Lett. 23, 40-42 (2002).
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