Cristiana Bolchini

Politecnico di Milano - Dip. Elettronica, Informazione e Bioingegneria - P.zza L. Da Vinci, 32 – 20133 Milano – Italy
@ cristiana.bolchini@polimi.it ☎ +39 0223993619 http://home.deib.polimi.it/bolchini/

Education

PhD, Automation and Computer Science Engineering, Politecnico di Milano, 1997.
Dissertation: "Quality issues in the design of digital systems.", Advisor: Prof. D. Sciuto

Laurea (5 years, equivalent to B.Sc and M.Sc), Electronic Engineering, Politecnico di Milano, (98/100) 1993.
Dissertation: "A support system for the design of easily testable VLSI architectures: design and implementation of an expert system for the application of Design-for-Testability techniques.", Advisor: Prof. M. G. Sami

Diploma Liceo Scientifico Liceo Scientifico Galileo Galilei, Caravaggio, (54/60) 1987.

High School Diploma, Mount Vernon High School, Mt. Vernon, MO, U.S.A., 1986.

Record of Employment

Professor ◇ *Politecnico di Milano* - Dip. Elettronica, Informazione e Bioingegneria ◇ Mar. 2015 - present.

Associate Professor ◇ *Politecnico di Milano* - Dip. Elettronica, Informazione e Bioing. ◇ Dec. 2003 - Mar. 2015.

Assistant Professor ◇ *Politecnico di Milano* - Dip. Elettronica e Informazione ◇ Sep. 1999 - Dec. 2003.

Research Assistant ◇ *Politecnico di Milano* - Dip. Elettronica e Informazione ◇ Mar. 1999 - Sep. 1999.

Scholarship student ◇ *CNR* ◇ Feb. 1998 - Jan. 1999.

Scholarship student ◇ *Politecnico di Torino* ◇ May 1997 - Apr. 1998.

PhD student ◇ *Politecnico di Milano* - Dip. Elettronica e Informazione ◇ Nov. 1993 - May 1997.

Consultant ◇ *Politecnico di Milano* - Dip. Elettronica e Informazione ◇ Feb. 1993 - Nov. 1993.

Editorial Services

Associate Editors-in-Chief ◇ *IEEE Transactions on Emerging Topics in Computing* ◇ Sep. 2013 - Apr. 2016.

Associate Editor ◇ *IEEE Transactions on Computers* ◇ Sep. 2007 - Oct. 2012.

Guest Editor for special issues/sections on reliability in IEEE Trans. on Computers, IEEE Trans. on Nanotechnology and other journals.

Academic Services/Responsibilities

Member of the Computer Science section board: 2013-present

Vice-head of the PhD board in Information Technology for the Computer Science section: 2016-2019

Member of the Committee for Abilitazione Scientifica Nazionale – SC 09/H1: 2016-2018

Rector's delegate for International Relationships with the Far East – Engineering: 2017-2019

IEEE Services

VP Financial ◇ *IEEE Council of EDA – CEDA* (CEDA) 2018-2019.

Member at large ◇ *IEEE Computer Society Publications Board – CS* (CS Pubs) 2019-present.

Professional Activities

Program-chair ◇ *DATE Conference* (DATE) 2020.

Vice Program-chair ◇ *DATE Conference* (DATE) 2019.

Track chair ◇ *T Test* (DATE) 2018.

Topic chair/co-chair ◇ *T4 System-Level Reliability Design, Analysis and On-line Test* (DATE) 2016-2017 / (DATE) 2015.

Tutorials Chair ◇ *DATE Conference* (DATE) 2016-2017

Friday Workshops Co-Chair ◇ *DATE Conference* (DATE) 2013-2015.

Workshop General Co-Chair ◇ *Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale* (MEDIAN) 2013.

Conference Finance Chair ◇ *Int. Conf. on Field Programmable Logic and Applications* (FPL) 2010.

Conference Program Co-Chair ◇ *IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems* (DFT) 2002 and 2007.

Conference General Co-Chair ◇ *IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems* (DFT) 2003 and 2008.

Technical Program Committee Membership ◇ IEEE/ACM Int. Conf. on Computer-Aided Design 2014 (ICCAD) ◇ Design Automation Conference 2012-2013 (DAC) ◇ IEEE/ACM Int. Conf. on Computer Design 2013-present (ICCD) ◇ IEEE/ACM Design and Test in Europe Conference, "On-Line Testing, Fault Tolerance, and Reliability" Track (DATE) 2004-2015 ◇ IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems (DFT) 2001-present ◇ IEEE Int. On-Line Testing Symp. (IOLTS) 2002-2009, 2011-2014 ◇ Euromicro Conf. on Digital System Design, Architectures, Methods and Tools, Special Session on "Dependability, Testing, and Fault Tolerance in Digital Systems" (DSD) 2008-present ◇ IEEE Int. Symp. Embedded Multicore/Many-core Systems-on-Chip (MCSoC) 2015-present ◇ HiPEAC Workshop on Reconfigurable Computing (WRC) 2016-present ◇ HiPEAC Workshop on Design for Reliability (DFR) 2010-2013.

Current and Recent International and National Projects

- EU FP7 STREP **SAVE** project "Self-Adaptive Virtualisation-Aware High-Performance/Low-Energy Heterogeneous System Architectures", coordinator (2013-2016).
- EU COST Action **MEDIAN** "ManufacturablE and Dependable multIcore Architectures at Nanoscale", co-Proponent and MC member (2011-2015).
- Italian National Technological Cluster 2014 - **EEB** - Zero Energy Buildings in Smart Urban Districts, (2014-2017).
- Regione Lombardia 2014 - **SCUOLA** - Smart Campus as Urban Open LAbs (2014-2016).
- European FP7 Strep Project - **FASTER** "Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration" (2011-2014).
- European Artemis Joint Undertaking **SMECY** "Smart Multicore Embedded SYstems", (2010-2012).
- Italian MIUR PRIN 2008 "High reliability fault tolerant digital systems in nanometric technologies: characterization and design methodologies", local scientific supervisor.
- European Artemis Joint Undertaking **SCALOPES** - "SCalable LOw Power Embedded platformS" (2009-2010).
- European ERC **SMSCom** - "Self-Managing Situated Computing" (2008-2013).
- Italian MIUR FIRB 2008 **ARTDECO** - "Adaptive infrastructures for decentralised organizations" (2006-2009).

Industrial/Other grants

- **Principal investigator** on Grant CG # 583539 from Cisco University Research Program Fund of Silicon Valley Community Foundation for "FIND2: A flexible functional diagnosis framework based on machine-learning techniques" - Oct. 2014/Sep.2015, US$100.000.
- **Principal investigator** on Grant CG #574830 from Cisco University Research Program Fund of Silicon Valley Community Foundation for "Exploiting (historical) test output data to improve functional diagnosis" - Jan. 2013/Dec.2013, US$100.000.
- **Co-Principal investigator** on Sponsored Research Agreement from Cisco Systems Inc. for "AFD (Automatic Fault Detective Analyzer)" - Jul. 2008/ Jul. 2009.
- **Co-principal advisor** on #NPI - ESA/ESTEC Contract 22079/08//NL/JK, for co-sponsored PhD on "Reliability-Aware Design Methodologies for Embedded Systems on Multi-FPGA Platforms" - Nov. 2008/Dec. 2011, EUR 90.000 (P.I.: Donatella Sciuto, PhD: Chiara Sandionigi).

Awards

- Best Paper Award "Reliability-Driven System-Level Synthesis of Embedded Systems," Proc. IEEE Int. Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems, 2010, pp. 35-43.
- Best Student Paper Award "A Reliable Reconfiguration Controller for Fault-Tolerant Embedded Systems on Multi-FPGA platforms," Proc. IEEE Intl Symp. Defect and Fault Tolerance in VLSI and Nanotechnology Systems, 2010, pp. 191-199.
- Best Paper Award Nominee "ReSP: A Non-Intrusive Transaction-Level Reflective MPSoC Simulation Platform for Design Space Exploration," Proc. IEEE 13th Asia and South Pacific Design Automation Conference (ASP-DAC), Seoul, Korea, 2008, pp. 673-678.
- Best Paper Award Nominee "Software methodologies for VHDL Code Static Analysis based on Flow Graphs," Proc. EuroDAC'96 with Euro-VHDL'96, (EuroVHDL) Geneve, Switzerland, 1996, pp. 406-411.

PhD Students Supervision

Angela Geronazzo ◇ *Data analysis for Energy Efficiency*, 2014-2017.

Matteo Carminati ◇ *Towards the Definition of a Methodology for the Design of Tunable Dependable Systems*, 2012-2014.

Chiara Sandionigi ◇ *A reliability-aware design methodology for embedded systems on multi-FPGA platforms*, 2009-2011.

Antonio Miele ◇ *A methodology for the design and analysis of reliable embedded systems*, 2007-2009.

Teaching Activity

PhD Level ◇ *Reliable Pervasive Computing Systems*, Politecnico di Milano, May 2007, May 2009 ◇ *Data management for context-aware, mobile systems*, Politecnico di Milano, May 2007, May 2009.

MSc Level ◇ *Dependable Systems*, Politecnico di Milano, 2012-present ◇ *Dependable Computing Systems*, Politecnico di Milano, 2005-2006, 2008-2010 ◇ *Operating Systems*, Politecnico di Milano, 2006-2008.

BSc Level ◇ *Digital Logic Design*, Politecnico di Milano, 2005-2014 ◇ *Fundamentals of Computer Science*, Politecnico di Milano, 1997-present.

Selected Publications

Summary: 39 refereed journal papers ◇ 9 editorial contributions ◇ 5 book chapters ◇ 105 refereed conference papers.
h-index: 26 ◇ **Total citations**: 2700 (source: Google Scholar, Feb. 2019)
The top five publications, according to Cristiana Bolchini, are highlighted.

¬ C. Bolchini, A. Geronazzo, E. Quintarelli, "Smart buildings: a monitoring and data analysis methodological framework" *Elsevier Building and Environment*, Vol. 121, (2017), pp. 93-105, (ISSN: 0360-1323)

¬ M.-H. Haghbayan, C. Bolchini, A. Miele, A. M. Rahmani, P. Liljeberg, A. Jantsch, and H. Tenhunen, "Can Dark Silicon Be Exploited to Prolong System Lifetime?" *IEEE Design & Test*, Vol. 34, No. 2, (2017), pp. 51-59, (ISSN: 2168-2356)

¬ C. Bolchini, L. Cassano, "A Fully Automated and Configurable Cost-Aware Framework for Adaptive Functional Diagnosis" *IEEE Design & Test*, Vol. 34, No. 2, (2017), pp. 79-86, (ISSN: 2168-2356)

¬ C. Bolchini, L. Cassano, "A Novel Approach to Incremental Functional Diagnosis for Complex Electronic Boards" *IEEE Trans. on Computers*, Vol. 65, no. 1, (2016), pp. 42-52, (ISSN: 0018-9340)

¬ C. Bolchini, L. Cassano, P. Garza, E. Quintarelli, F. Salice, "An Expert CAD Flow for Incremental Functional Diagnosis of Complex Electronic Boards" *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems*, Vol. 34, No. 5, (2015), pp. 835-848, (ISSN: 0278-0070)

¬ C. Bolchini, C. Sandionigi, "Design of Hardened Embedded Systems on Multi-FPGA Platforms" *ACM Trans. on Design Automation of Electronic Systems*, Vol. 20, no. 1, (2014), pp. 16:1–16:26, (ISSN: 1084-4309)

¬ C. Bolchini, A. Miele, C. Sandionigi, "Autonomous fault-tolerant systems onto SRAM-based FPGA platforms" *Journal of Electronic Testing - Theory and Applications, Springer*, Vol. 29, No. 6, (2013), pp. 779-793, (ISSN: 0923-8174)

¬ C. Bolchini, A. Miele, "Reliability-driven System-level Synthesis for Mixed-Critical Embedded Systems" *IEEE Trans. on Computers,* Vol. 62, no. 12 (2013), pp. 2489-2502, (ISSN: 0018-9340)

¬ C. Bolchini, M. Carminati, A. Miele, "Self-Adaptive Fault Tolerance in Multi-/Many-Core Systems" *Journal of Electronic Testing - Theory and Applications, Springer* Vol. 29, no. 2, (2013), pp. 159-175, (ISSN: 0923-8174)

¬ C. Bolchini, E. Quintarelli, L. Tanca, "CARVE: Context-aware automatic view definition over relational databases" *Information Systems, Elsevier* Vol. 38, no. 1, (2013), pp. 45-67, (ISSN: 0306-4379)

¬ C. Bolchini, A. Miele, C. Sandionigi, "A Novel Design Methodology for Implementing Reliability-Aware Systems on SRAM-Based FPGAs," *IEEE Trans. on Computers,* Vol. 60, No. 12, (2011), pp. 1744-1758, (ISSN: 0018-9340)

– S. Montanelli D. Bianchini, C. Aiello, R. Baldoni, C. Bolchini, S. Bonomi, S. Castano, T. Catarci, V. De Antonellis, A. Ferrara, M. Melchiori, E. Quintarelli, M. Scannapieco, F. A. Schreiber, L. Tanca, "The ESTEEM platform: enabling P2P semantic collaboration through emerging collective knowledge," *Journal of Intelligent Information Systems, Springer,* Vol. 36, no. 2, (2011), pp. 167-195 (ISSN: 0925-9902)

¬ C. Bolchini, C. Sandionigi, "Fault Classification for SRAM-Based FPGAs in the Space Environment for Fault Mitigation," *IEEE Embedded Systems Letters,* Vol. 2, no. 4, (2010), pp. 107-110 (ISSN: 1943-0663)

– D. Bianchini, S. Montanelli, C. Aiello, R. Baldoni, C. Bolchini, S. Bonomi, S. Castano, T. Catarci, V. De Antonellis, A. Ferrara, M. Melchiori, E. Quintarelli, M. Scannapieco, F. A. Schreiber, L. Tanca, "Emergent Semantics and Cooperation in Multi-knowledge Communities: the ESTEEM Approach," *World Wide Web, Springer* Vol. 13, no. 1-2, (2010), pp. 3-31 (ISSN: 1386-145X)

¬ L. Amati, C. Bolchini, F. Salice, F. Franzoso, "Improving Fault Diagnosis Accuracy by Automatic Test Set Modification," *Proc. IEEE Int. Test Conference* (ITC), Austin, USA, 2010, pp. 16.2-1–16.2-8.

¬ C. Bolchini, A. Miele, "Reliability-Driven System-Level Synthesis of Embedded Systems," *Proc. IEEE Intl. Symp. on Defect and Fault Tolerance in VLSI Systems* (DFT), Kyoto, J, 2010, pp. 35–43. **Best Paper Award**

¬ C. Bolchini, C. A. Curino, G. Orsi, E. Quintarelli, R. Rossato, F. A. Schreiber, L. Tanca, "And what can context do for data?," *Communications of the ACM,* Vol. 52, no. 11, (2009), pp. 136–140. (ISSN: 0001-0782)

¬ C. Bolchini, C. A. Curino, E. Quintarelli, F. A. Schreiber, L. Tanca, "Context Information for Knowledge Reshaping," *Int. J. of Web Engineering and Technology,* Special Issue on Web-based Knowledge Representation and Management*,* Vol. 5, no. 1, (2009), pp. 88–103. (ISSN: 1476-1289)

– C. Bolchini, A. Miele, M. Rebaudengo, F. Salice, D. Sciuto, L. Sterpone, M. Violante, "Software and Hardware Techniques for SEU Detection in IP Processors," *Journal of Electronic Testing: Theory and Applications, Springer,* Vol. 24, no. 1-3, (2008), pp. 35–44. (ISSN: 0923-8174)

– C. Bolchini, C. A. Curino, E. Quintarelli, F. A. Schreiber, L. Tanca, "A Data-oriented Survey of Context Models," *ACM SIGMOD Record,* Vol. 36, no 4, (2007), pp. 19–26. (ISSN:0163-5808)

– C. Bolchini, F. A. Schreiber, L. Tanca, "A methodology for a Very Small Data Base design," *Information Systems, Elsevier,* Vol. 32, no. 1, (2007), pp. 61–82. (ISSN:0306-4379)

– C. Bolchini, P. Ferrandi, P. L. Lanzi, F. Salice, "Evolving Classifiers on Field Programmable Gate Arrays: Migrating XCS to FPGAs," *Journal of System Architecture, Special issue on Nature Inspired Applied Systems, Elsevier* Vol. 52, no. 8-9, (2006), pp. 516–533 (ISSN:1383-7621)

– C. Bolchini, F. A. Schreiber, L. Tanca, "A context-aware methodology for very small data base design," *ACM SIGMOD Record,* Vol. 33, no 1, (2004), pp. 71–76. (ISSN:0163-5808)

– C. Bolchini, "A Software Methodology for Detecting Hardware Faults in VLIW Data Paths," *IEEE Trans. on Reliability,* (TR) Vol. 52, no. 4, (2003), pp. 458–468. (ISSN: 0018-9529/03)

¬ C. Bolchini, F. Salice, F. A. Schreiber, L. Tanca, "Logical and Physical Design Issues for Smart Card Databases," *ACM Trans. on Information Systems,* (TOIS), Vol. 21, no. 3, (2003), pp. 254–285. (ISSN: 1046-8188)

¬ C. Bolchini, L. Pomante, F. Salice, D. Sciuto, "The Design of Reliable Devices for Mission Critical Applications," *IEEE Trans. on Instrumentation and Measurement,* (TIM) Vol. 52, no. 6, (2003), pp. 1703–1712. (ISSN: 0018-9456/03)

Last update: Feb. 2019