Curriculum Vitæ et Studiorum

Name	GIANLUCA PALERMO
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Short Bio

He received the M.S degree in Electronic Engineering, in 2002, and the Ph.D degree in Computer Engineering, in 2006, from Politecnico di Milano. He is currently an Associate Professor with tenure at Department of Electronics, Information and Bioengineering in the same University. Previously he was consultant engineer in the Low Power Design Group of AST - STMicroelectronics (Agrate, Italy) working on network on-chip and research assistant at the Advanced Learning and Research Institute (ALaRI) of the Universita' della Svizzera Italiana (Lugano, Switzerland). His research interests include design methodologies and architectures for Embedded and High Performance Computing systems, focusing on multi/many-cores architectures, and application autotuning. Since 2003, he published over 100 peer-reviewed papers including top-level conferences and journals ($>$ 2500 total citations and h-index of 25 according to Google Scholar).

Contents

Position and Education

RECORD OF EMPLOYMENT

05/2015 – present

Associate Professor with tenure in Computer Engineering at the Department of Electronics, Information and Bioengineering (DEIB) of the Politecnico di Milano.

05/2008 – 05/2015

Assistant Professor (MIUR) with tenure in Computer Engineering at the Department of Electronics, Information and Bioengineering (DEIB) of the Politecnico di Milano.

03/2003–04/2008

Post-Doctoral Researcher at the Department of Electronics and Information (DEI) of the Politecnico di Milano working on "Low Power Network on Chip and Multiprocessor Platforms".

04/2006–09/2007

Research fellow at Advanced Learning and Research Institute (ALaRI) of the USI - Universita' della Svizzera Italiana working on Network on-Chip design methodologies and architectures in the context of the European project *MEDEA+ - LoMoSa: Low Power expertise for Mobile and multi-media System Applications*.

04/2002–03/2003

Consultant engineer at the Low Power Design Group of AST - R&I (Advanced System Technology - Research and Innovation) - STMicroelectronics working on Network on-Chip architectures in the context of the European project *MEDEA+ - Silicon Application Platform for Pocket Multimedia.*

EDUCATION

- Ph.D. in Information Technology at Politecnico di Milano in 2006.
  Thesis Title: *Design Methodologies for Embedded Architectures based-on Network-on-Chip*
  Advisor: *Prof. Cristina Silvano*
  Reviewer: *Marcello Coppola, Head of the AST - STMicroelectronics Lab in Grenoble*
  Award: *Dimitris N. Chorafas Foundation* - Carlo Pesenti Prize

- *Laurea* Degree in Electronic Engineering in 2002
  Thesis title: *Una metodologia di esplorazione architetturale e di codifica dell'informazione per sistemi digitali a bassa dissipazione di potenza*,
  Advisor: *Prof. Mariagiovanna Sami*

VISITING EXPERIENCES

- Visiting researcher at STMicroelectonics Grenoble (July-2005 to August-2005)
- Visiting researcher at STMicroelectonics Grenoble (July-2006)

Awards

AW.1. Dimitris N. Chorafas Foundation, Carlo Pesenti prize for the PhD thesis.

AW.2. HiPEAC Paper Award as co-author of the paper - Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Aleksandar Brankovic, Jovana Jovic, Cristina Silvano. "A Correlation-Based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip " DAC - Design Automation Conference, Anheim, CA, USA, 2010

Professional Activities

Scientific Committees

- Chair of the panel for the *Academy of Finland* - Call 2018 - Electronics and Electrical Engineering
- Panel member for the *Academy of Finland* - Call 2017 - Energy-Efficient ICT Systems of the Future
- Panel member for the *Academy of Finland* - Call 2016 - Electronics and Electrical Engineering
- Proposal reviewer for Singapore Ministry of Education (MOE) - Call 2015
- Panel member for the *Academy of Finland* - Call 2013 - Electronics and Processor Architectures
- Reviewer for the *French National Research Agency (ANR)* - Call 2013
- Panel member for the *Academy of Finland* - Call 2012 - Electronics and Processor Architectures

Contribution to National and International Research Projects

- *H2020-FETHPC-671623-ANTAREX: AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems (FET Project)*
  Local project leader: Prof. Cristina Silvano (POLIMI)
  Role: Co-applicant, Task Leader and Research Team Member (Level of involvement: HIGH)
  Activities: Development of a self-adaptive application-level framework for energy efficient execution in HPC platforms. The framework exploits autonomous and and approximate computing concepts by tuning application-level knobs according to dynamically changing functional and extra-functional requirements. He was co-applicant of the project.
- *FP7-ICT-611146-CONTREX : Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties (IP Project)*
  Local project leader: Prof. William Fornaciari (POLIMI)
  Role: Co-applicant, Task Leader and Research Team Member (Level of involvement: HIGH)
  Activities: Design and implementation of (i) a multi-level design space exploration framework for real-time embedded system and (ii) an application-level run-time monitoring framework for the extra functional properties. He was co-applicant of the project.
- *FP7-ICT-247999-COMPLEX : CO-design and power Management in PLatform-based design space Exploration (IP Project)*
  Local project leader: Prof. William Fornaciari (POLIMI)
  Role: Co-applicant, Task Leader and Research Team Member (Level of involvement: HIGH)
  Activities: Definition and implementation of power-aware methodologies in a model-driven HW/SW co-design flow based on the introduction of an automatic design space exploration engine.

- *FP7-ICT-248716-2PARMA : PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures (STREP Project)*
  Local project leader: Prof. Cristina Silvano (POLIMI) - Co-applicant of the Project
  Role: Co-applicant and Research Team Member (Level of involvement: MEDIUM)
  Activities: Implementation of an application-specific run-time manager to support application adaptation on multi/many-core architectures. He was co-applicant of the project.

- *ARTEMIS-100230-SMECY : Smart Multicore Embedded SYstems*
  Local project leader: Prof. Donatella Sciuto (POLIMI)
  Role: Research Team Member (Level of involvement: MEDIUM)
  Activities: Definition and implementation of design space exploration techniques to statically support the a system-wide run-time resource manager on a many-core architecture (ST-P2012/STHORM).

- *FP7-ICT-216693-MULTICUBE : MULTI-objective Design Space Exploration of MULTIprocessor SOC Architectures for Embedded MULTImedia Applications (STREP project)*
  Local project leader: Prof. Cristina Silvano (POLIMI)
  Role: Co-applicant, Work-Package Leader and Deputy Project Coordinator (Level of involvement: HIGH)
  Activities: Coordinator of all the project activities regarding the automatic design space exploration (A-DSE) of multiprocessor architectures. Development of an A-DSE tool in terms of design of experiment modules, exploration algorithms and response surface models. He was co-applicant of the project.

- *Medea+-2A708-LoMoSa: Low Power expertise for Mobile and multi-media System Applications*
  Local project leader: Prof. Mariagiovanna Sami (ALaRI-USI)
  Role: Co-applicant, Task Leader and Research Team Member (Level of involvement: HIGH)
  Activities: Analysis and implementation of low-level security services and power-aware design techniques for the ST-NoC communication architecture. He was co-applicant of the project.

- *Low Power Network on Chip and Multiprocessor Platforms (STM/POLIMI project)*
  Local project leader: Prof. Cristina Silvano (POLIMI)
  Role: Task Leader and Research Team Member (Level of involvement: HIGH)
  Activities: Analysis and optimization of the synchronization problem in NoC-based multiprocessors. Definition of power-aware policies for the on-chip interconnection.

- *FP6-IST-035143-hARTES: Holistic Approach to Reconfigurable Real-Time Embedded Systems (IP Project)*
  Local project leader: Prof. Donatella Sciuto (POLIMI)
  Role: Research Team Member (Level of involvement: LOW)
  Activity: Design and analysis of a reconfigurable multiprocessor platform (called *CERBERO*) to internally validate an high-level HW-SW partitioning and mapping tool.

- *MIUR FIRB MAIS Multichannel Adaptive Information Systems*
  Local project leader: Prof. Barbara Pernici (POLIMI)
  Role: Research Team Member (Level of involvement: LOW)
  Activities: Design and implementation of power estimation (SW oriented) and optimization techniques (architecture-oriented) for the low-power LX-VLIW architectures designed by STMicroelectronics.

- *Low Power Network on Chip and Embedded Architectures (STM/POLIMI project)*
  Local project leader: Prof. Cristina Silvano (POLIMI)
  Role: Research Team Member (Level of involvement: HIGH)
  Activities: Design and Implementation of an on-chip interconnection architecture for embedded systems based on a pure NoC philosophy. Analysis of the NoC-based Hyperprocessor architecture designed by STMicroelectronics from a power/performance/programmability point of view.

- *Medea+-A207 - Pocket Multimedia - Silicon Application Platform for Pocket Multimedia*
  Local project leader: Roberto Zafalon (STM)
  Role: Research Team Member (Level of involvement: MEDIUM)
  Activities: Design and implementation of power estimation techniques for the ST-BUS architecture based on gate level analysis.

CONFERENCE AND WORKSHOP ORGANIZATION

Program Chair

- ReC4P - International Workshop on Reconfigurable Computing for HPC and HPDA - (2015)
- RAPIDO - International Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools - (2013 – 2017, 2019)

Steering Committees

- CF - Computing Frontiers - *Steering Committee member* (2017 - 2019)

Organizing Committees

- CF - Computing Frontiers - *General Chair* (2016), *Registration Chair* (2017), *Workshop Chair* (2019)
- ANDARE - Workshop on AutotuniNg and aDaptivity AppRoaches for Energy efficient HPC Systems - Co-located with PACT - *Publicity Chair* (2017, 2018)
- ReC4P - International Workshop on Reconfigurable Computing for HPC and HPDA - *Organizing Committee* (2015)
- RAPIDO - International Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools - *Organizing Committee* (2013 - 2019)
- ARCS - International Conference on Architecture of Computing Systems - *Publicity Chair and Local Committee* (2011)
- MICRO - International Symposium on Microarchitecture - *Local Arrangements Chair* (2008)

Track/Topic Chair

- CODES+ISSS - International Conference on Hardware/Software Codesign and System Synthesis - *Track Chair on System Level Design* - 2017
- EUC - International Conference on Embedded and Ubiquitous Computing - *Track Chair on Power Efficient Computing* - 2014
- PARMA - International Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures - *Track Chair on Design Space Exploration and Many-core Architecture Customization* - 2010, 2011

Program Committee Membership

- DATE (2006 – 2010, 2015 – 2019) - Design Automation and Test in Europe.
  - In 2017 and 2019 member of the special committee for the *Best Interactive Presentation Award*.
- CODES+ISSS (2017–2019) - International Conference on Hardware/Software Codesign and System Synthesis
- ReConFig (2016–2018) - International Conference on ReConFigurable Computing and FPGAs
- FPL (2015 – 2019) - International Conference on Field-Programmable Logic and Applications
- ASAP (2018) - International Conference on Application-specific Systems, Architectures and Processors
- CF (2012, 2015) - International Conference on Computing Frontiers
- IC-SAMOS (2015 – 2019) - International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
- EUC (2005, 2014 – 2015) - International Conference on Embedded and Ubiquitous Computing
- MCSoC (2014 – 2019) - International Symposium on Embedded Multicore/Many-core Systems-on-Chip
- RAPIDO (2011 – 2019) - International Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools
- IA^3 (2011 – 2017) - International Workshop on Irregular Applications: Architectures and Algorithms
- CS^2 (2014, 2015) - International Workshop Cryptography and Security in Computing Systems
- MOMAC (2014 – 2016) - International Workshop on Multi-Objective MAny-Core design
- MES (2013 – 2017) - International Workshop on Many-core Embedded Systems
- WRC (2013 – 2017) - International Workshop on Reconfigurable Computing
- PARMA-DITAM (2014 – 2018) - Joint International Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and on Design Tools and Architectures for Multi-Core Embedded Computing Platforms
- OPTIM (2016–2019) - International Workshop on Optimization Issues in Energy Efficient HPC & Distributed Systems
- ANDARE (2017–2018) - Workshop on AutotuniNg and aDaptivity AppRoaches for Energy efficient HPC Systems
- NoCArc (2008 – 2016) - International Workshop on Network on Chip Architectures
- AASC (2015) - International Workshop on Architecture-Aware Simulation and Computing
- PARMA (2010 – 2013) - International Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures
- SOC (2012) - International Symposium on System-on-Chip
- CDES (2007) - International Conference on Computer Design
- ESA (2007) - International Conference on Embedded Systems and Applications

REFEREE SERVICES IN JOURNALS AND CONFERENCES

- *Conferences and Workshops*: DAC - Design Automation Conference, MICRO - International Symposium on Microarchitecture, ARCS - International Conference on Architecture of Computing Systems, DATE - Design Automation and Test in Europe, ICCAD - International Conference on Computer Aided Design, PATMOS - International Workshop on Power and Timing Modelling, SAC - Symposium on Applied Computing, EUC - Embedded and Ubiquitous Computing, SAMOS - International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, FPL - International Conference on Field Programmable Logic and Applications, VLSI-SoC - IFIP/IEEE International Conference on Very Large Scale Integration, International Symposium on System-on-Chip, ACM International Conference on Computing Frontier, ACM/IEEE International Symposium on Networks-on-Chip, IEEE Symposium on Application Specific Processors (SASP), HiPEAC - International conference on High-Performance Embedded Architectures and Compilers, ICPP - International Conference on Parallel Processing, ISCAS - International Symposium on Circuits and Systems.

- *Journals*: IEEE Transactions on Computers (TC), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Very Large Scale Integration Systems (TVLSI), ACM Transactions on Embedded Computing Systems (TECS), ACM Transactions on Design Automation of Electronic Systems (TODAES), ACM Transactions on Architecture and Code Optimization (TACO), IEEE Transactions on Cybernetics (TCYB), IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE Computer Architecture Letters (CAL), IEEE Transactions on Multi-Scale Computing Systems (TMSCS), ELSEVIER Microprocessors and Microsystems: Embedded Hardware Design (MICPRO), ELSEVIER Journal of System Architecture (JSA), ELSEVIER Computers & Electrical Engineering (COMPELECENG), SPRINGER Design Automation for Embedded Systems (DAES), SPRINGER Optimization Letters (OL), SPRINGER Journal of Supercomputing (JSUPE), IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), IEEE Embedded Systems Letters (ESL), IET Computers & Digital Techniques (IET-CDT), SPRINGER Journal of Computer Science and Technology (JCST), MDPI - Journal of Low Power Electronics and Applications (JLPEA), ELSEVIER Simulation Modelling Practice and Theory (SIMPAT)

Teaching Activities

Course Responsibility

- Computing Systems - (10 credits)
  Politecnico di Milano - Engineering Physics - Graduate level
  Academic Years: 18/19
- Computing Systems for Engineering Physics - (10 credits)
  Politecnico di Milano - Engineering Physics - Graduate level
  Academic Years: 15/16, 16/17, 17/18
- Reti Logiche - (5 credits)
  Politecnico di Milano - Computer Engineering - Undergraduate level
  Academic Years: 15/16, 16/17, 17/18, 18/19
- Prova Finale (Progetto di Reti Logiche) - (1 credit)
  Politecnico di Milano - Computer Engineering - Undergraduate level
  Academic Years: 17/18, 18/19
- Informatica ed Elementi di Informatica Medica [1] (7 credits)
  Politecnico di Milano - Biomedical Engineering - Undergraduate level
  Academic Years: 09/10, 10/11, 11/12, 12/13, 13/14, 14/15
- Informatica B - Informatica per Applicazioni Scientifiche e Industriali (10 credits)
  Politecnico di Milano - Engineering Physics - Graduate level
  Academic Years: 12/13, 13/14, 14/15
- Metodologie di Progetto Hardware/Software (5 credits)
  Politecnico di Milano - Computer Engineering - Graduate level
  Academic Year: 09/10
- Sistemi Informatici (7 credits)
  Politecnico di Milano - Automation Engineering - Undergraduate level
  Academic Year: 08/09
- Cultura Tecnologica di Progetto - Informatica (2.5 credits)
  Politecnico di Milano - Product Design - Undergraduate level
  Academic Year: 07/08
- Design Laboratory 2 (3 credits)
  ALaRI - Universita' della Svizzera Italiana - Embedded System Design - Graduate level
  Academic Years: 05/06, 06/07, 07/08
- Progettazione VLSI per il consumo di potenza, l'area e le prestazioni (shared with F. Ferrandi)
  Politecnico di Milano - Information Technology PhD - PhD level
  Academic Year: 06/07

Teaching Assistant

- Informatica ed Elementi di Informatica Medica [1] (24h)
  Politecnico di Milano - Biomedical Engineering - Undergraduate level
  Course Responsible: Prof. Manuel Roveri
  Academic Years: 15-16, 16-17, 17-18

- Reti Logiche A (20h)
  Politecnico di Milano - Computer Engineering - Undergraduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Years: 10-11, 09-10, 08-09, 07-08, 06-07, 05-06, 04-05, 03-04

- Reti Logiche B (20h)
  Politecnico di Milano - Electronic Engineering - Undergraduate level
  Course Responsible: Prof. Fabrizio Ferrandi and Prof. Mariagiovanna Sami
  Academic Years: 08-09, 07-08, 06-07, 05-06, 04-05, 03-04

- Metodologie di Progetto Hardware e Laboratorio (20h)
  Politecnico di Milano - Computer Engineering - Graduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Years: 07-08, 06-07, 05-06, 04-05

- Metodologie di Progetto Hardware (10h)
  Politecnico di Milano - Computer Engineering - Graduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Year: 03-04

- Laboratorio di Metodologie di Progetto Hardware (10h)
  Politecnico di Milano - Computer Engineering - Graduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Year: 03-04

- Calcolatori Elettronici A (20h)
  Politecnico di Milano - Computer Engineering - Undergraduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Year: 02-03

- Calcolatori Elettronici (40h)
  Politecnico di Milano - Electronic and Telecommunication Engineering - Graduate
  Course Responsible: Prof. Cristina Silvano
  Academic Years: 02-03, 01-02

STUDENTS' SUPERVISION

PhD Students Supervision

- *Marco Ceriani - Advisor*, 2010–2014
  Title: "Design Methodologies and Multiprocessor Architectures for Irregular HPC Applications"

- *Ioannis Stamelakos - Co-Advisor*, 2012–2016
  Title: "Technology-Aware Many-core Architecture Design"

- *Amir H. Ashouri - Co-Advisor*, 2012–2016
  Title: "Compiler Auto-Tuning for Embedded Computing Platforms"

- *Davide Gadioli - Advisor*, 2014–2019
  Title: "Dynamic Application AutoTuning for Self-Aware Approximate Computing"

- *Emanuele Vitali- Advisor*, 2017–present
  Title: "Mixed Design-time/Run-time Approaches to Application AutoTuning in Heterogeneous Architectures"

Graduate Students Supervision/Co-Advisor

- He advised and co-advised more than 30 students within Politecnico di Milano, ALaRI - USI and STMicrolectronics facilities.

Publication List

PATENTS

PA.1. Valerio Catalano, Riccardo Locatelli, Marcello Coppola, Gianluca Palermo, Leandro Fiorin, Cristina Silvano, "Programmable Data Protection Device, Secure Programming Manager System and Process For Controlling Access to an Interconnect Network for an Integrated Circuit". US Patent Office publication number: US2009089861 (B2).

PA.2. Valerio Catalano, Riccardo Locatelli, Marcello Coppola, Gianluca Palermo, Leandro Fiorin, Cristina Silvano, "Programmable Data Protection Device, Secure Programming Manager System and Process For Controlling Access to an Interconnect Network for an Integrated Circuit". European Patent Office publication number: EP2043324 (A1).

REFEREED INTERNATIONAL JOURNALS

JR.1. Stamelakos Ioannis, Xydis Sotirios, Palermo Gianluca, Silvano Cristina. "Workload- and Process-Variation Aware Voltage/Frequency Tuning for Energy Efficient Performance Sustainability of NTC Manycores". *Integration, the VLSI Journal*. Accepted for publication. 2018.

JR.2. Davide Gadioli, Emanuele Vitali, Gianluca Palermo, Cristina Silvano: mARGOt: A Dynamic Autotuning Framework for Self-Aware Approximate Computing. *IEEE Transactions on Computers*. Volume 68 Issue 5, pp. 713-728, 2019. DOI: https://doi.org/10.1109/TC.2018.2883597

JR.3. Amir H. Ashouri, William Killian, John Cavazos, Gianluca Palermo, Cristina Silvano. "A Survey on Compiler Autotuning using Machine Learning" *ACM Computing Surveys*. Volume 51, Issue 5. pp 96:1-96:42. 2019
DOI: https://doi.org/10.1145/3197978

JR.4. Amir H. Ashouri, Andrea Bignoli, Gianluca Palermo, Cristina Silvano, Sameer Kulkarni, and John Cavazos. "MiCOMP: Mitigating the Compiler Phase-Ordering Problem Using Optimization Sub-Sequences and Machine Learning". *ACM Transactions on Architecture and Code Optimization*. Volume 14, Issue 3, Article 29 (September 2017), 28 pages.
DOI: https://doi.org/10.1145/3124452

JR.5. Marco Ceriani, Simone Secchi, Oreste Villa, Antonino Tumeo, Gianluca Palermo. "Exploring Efficient Hardware Support for Applications with Irregular Memory Patterns on Multinode Manycore Architectures", *IEEE Transactions on Parallel and Distributed Systems*. Volume 28, Issue 6 (June 2017), 1635-1648.
DOI: https://doi.org/10.1109/TPDS.2014.2345073

JR.6. Gruttner Kim, Gorgen Ralph, Schreiner Sren, Herrera Fernando, Penil Pablo, Medina Julio, Villar Eugenio, Palermo Gianluca, Fornaciari William, Brandolese Carlo, Gadioli Davide, Vitali Emanuele, Bocchio Sara, Ceva Luca, Azzoni Paolo, Poncino Massimo, Vinco Sara, Macii Enrico, Cusenza Salvatore, Favaro John, Valencia Raul, Sander Ingo, Rosvall Kathrin, Khalilzad Nima, Quaglia Davide. "CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties". *Microprocessors and Microsystems* Vol. 51, 2017. pp. 39–55, ISSN: 0141-9331. DOI: 10.1016/j.micpro.2017.03.012

JR.7. Amir Hossein Ashouri, Giovanni Mariani, Gianluca Palermo, Eunjung Park, John Cavazos, and Cristina Silvano. "COBAYN: Compiler Autotuning Framework using Bayesian Networks". *ACM Transactions on Architecture and Code Optimization*. Volume 13, Issue 2, Article 21 (June 2016), 25 pages.
DOI: http://dx.doi.org/10.1145/2928270

JR.8. Parinaz Sayyah, Mihai T. Lazarescu, Sara Bocchio, Gianluca Palermo, Davide Quaglia, Alberto Rosti, Luciano Lavagno. "Virtual Platform-based Design Space Exploration of Power-Efficient Distributed Embedded Applications", *ACM Transactions on Embedded Computing Systems*. Volume 14 Issue 3, Article 49, May 2015.

JR.9. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "DESPERATE++: An Enhanced Design Space Exploration Framework using Predictive Simulation Scheduling", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Volume 34, no. 2, pp. 293-306, Feb. 2015.

JR.10. Sotirios Xydis, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High Level Synthesis", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Volume 34, no. 1, pp. 155-159, Jan. 2015.

JR.11. Leandro Fiorin, Gianluca Palermo and Cristina Silvano. "A Configurable Monitoring Infrastructure for NoC-based Architectures", *IEEE Transactions on VLSI Systems*. vol. 22, no. 11, pp. 2438-2442, Nov. 2014.

JR.12. Fernando Herrera, Hector Posadas, Pablo Penil, Eugenio Villar, Francisco Ferrero, Raul Valencia and Gianluca Palermo. "The COMPLEX Methodology for UML/MARTE Modelling and Design Space Exploration of Embedded Systems" *Elsevier - Journal of System Architectures*, Volume 60, Issue 1 (January 2014), 55-78.

JR.13. Kim Gruttner, Philipp A. Hartmann, Kai Hylla, Sven Rosinger, Wolfgang Nebel, Fernando Herrera, Eugenio Villar, Carlo Brandolese, William Fornaciari, Gianluca Palermo, Chantal Ykman-Couvreur, Davide Quaglia, Francisco Ferrero, Raul Valencia. "The COMPLEX reference framework for HW/SW Co-Design and Power Management Supporting Platform-Based Design-Space Exploration" *Elsevier Journal - Microprocessors and Microsystems: Embedded Hardware Design*. Volume 37, Issue 8, Part C, November 2013, Pages 966–980.

JR.14. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria and Cristina Silvano. "Design Space Exploration and Run-time Resource Management for Multi-cores", *ACM Transactions on Embedded Computing Systems*. Volume 13 Issue 2, September 2013, Article No. 20.

JR.15. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria and Cristina Silvano. "ARTE: an Application-specific Run-Time Management Framework for Multi-cores based on Queuing Models", *Elsevier Journal - Parallel Computing*, Volume 39 (2013), pp. 504-519.

JR.16. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "A Variability-Aware Robust Design Space Exploration Methodology for CMPs", *ACM Transactions on Embedded Computing Systems*. Volume 11, Issue 2, July 2012, pp. 29.1-29.28.

JR.17. Giovanni Mariani, Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Spaces", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Volume 21 Issue 5, May 2012, pp. 740-753.

JR.18. Chantal Ykman-Couvreur, Prabhat Avasare, Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "Linking run-time resource management of embedded multi-core platforms with automated design-time exploration", *IET Computers and Digital Techniques*. Vol. 5. Issue 2, 2011, pp. 123-135.

JR.19. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "ReSPIR: A Response Surface-based Pareto Iterative Refinement for Application-Specific Design Space Exploration", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Volume 28 Issue 12, December 2009 pp. 1816-1829.

JR.20. Christian Pilato, Antonino Tumeo, Gianluca Palermo, Fabrizio Ferrandi, PierLuca Lanzi and Donatella Sciuto. "Improving Evolutionary Exploration to Area-Time Optimization of FPGA Designs", *Journal of System Architectures, Elsevier*. Volume 54, Issue 11, November 2008, Pages 1046-1057

JR.21. Leandro Fiorin, Gianluca Palermo, Cristina Silvano and Valerio Catalano. "Secure Memory Accesses on Network-on-Chip", *IEEE Transactions on Computers*. Volume 57 Issue 9, September 2008 pp. 1216-1229.

JR.22. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "Exploration of Distributed Shared Memory Architectures for NoC-based Multiprocessors", *Journal of System Architectures, Elsevier*. Volume 53, Issue 10, October 2007 pp. 719-732.

JR.23. Giovanni Agosta, Gianluca Palermo, Cristina Silvano. "Efficient Architecture/Compiler Co-Exploration Using Analytical Models", *Design Automation for Embedded Systems*, Springer, Volume 11, Issue 1, March 2007, pp. 1-23.

JR.24. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "Efficient Synchronization for Embedded on-Chip Multiprocessors", *IEEE Transactions on VLSI Systems*. Volume 14 Issue 10, October 2006 pp. 1049-1062.

JR.25. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "An Efficient Synchronization Technique for Multiprocessor Systems on-Chip", *ACM SIGARCH Computer Architecture News*, Volume 34 , Issue 1 (March 2006) pp. 33-40.

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