Curriculum Vitæ et Studiorum

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Short Bio

He received the M.S degree in Electronic Engineering, in 2002, and the Ph.D degree in Computer Engineering, in 2006, from Politecnico di Milano. He is currently an Associate Professor with tenure at Department of Electronics, Information and Bioengineering in the same University. Previously, he was consultant engineer in the Low Power Design Group of AST - STMicroelectronics (Agrate, Italy) working on network on-chip and research assistant at the Advanced Learning and Research Institute (ALaRI) of the Universita' della Svizzera Italiana (Lugano, Switzerland). His research interests include design methodologies and architectures for Embedded and High Performance Computing systems, focusing on multi/many-cores architectures, application autotuning, and high throughput virtual screening. Since 2003, he published over 150 peer-reviewed papers including top-level conferences and journals ($>$ 3700 total citations and h-index of 32 according to Google Scholar). He is ACM, HiPEAC and EuroLab4HPC member, IEEE senior member and PoliMi representative within EIT Digital.

Contents

Position and Education

RECORD OF EMPLOYMENT

05/2015 – present

Associate Professor with tenure in Computer Engineering at the Department of Electronics, Information and Bioengineering (DEIB) of the Politecnico di Milano.

05/2008 – 05/2015

Assistant Professor (MIUR) with tenure in Computer Engineering at the Department of Electronics, Information and Bioengineering (DEIB) of the Politecnico di Milano.

04/2006–04/2008

Post-Doctoral Researcher at the Department of Electronics and Information (DEI) of the Politecnico di Milano working on "Low Power Network on Chip and Multiprocessor Platforms".

04/2006–09/2007

Research fellow at Advanced Learning and Research Institute (ALaRI) of the USI - Universita' della Svizzera Italiana working on Network on-Chip design methodologies and architectures in the context of the European project *MEDEA+ - LoMoSa: Low Power expertise for Mobile and multi-media System Applications*.

07/2005–08/2005, 07/2006

Visiting researcher at STMicroelectonics, AST - R&I (Advanced System Technology - Research and Innovation), Grenoble, France, working on power modeling in the context of Network on-Chip architectures.

03/2003–03/2006

Research Assistant at the Department of Electronics and Information (DEI) of the Politecnico di Milano working on "Low Power Network on Chip and Multiprocessor Platforms".

04/2002–03/2003

Consultant engineer at the Low Power Design Group of AST - R&I (Advanced System Technology - Research and Innovation) - STMicroelectronics working on Network on-Chip architectures in the context of the European project *MEDEA+ - Silicon Application Platform for Pocket Multimedia.*

EDUCATION

- Ph.D. in Information Technology at Politecnico di Milano in 2006.
  Thesis Title: *Design Methodologies for Embedded Architectures based-on Network-on-Chip*
  Advisor: *Prof. Cristina Silvano*
  Award: *Dimitris N. Chorafas Foundation* - Carlo Pesenti Prize

- *Laurea* Degree in Electronic Engineering in 2002
  Thesis title: *Una metodologia di esplorazione architetturale e di codifica dell'informazione per sistemi digitali a bassa dissipazione di potenza*,
  Advisor: *Prof. Mariagiovanna Sami*

Awards

AW.1. Dimitris N. Chorafas Foundation, Carlo Pesenti prize for the PhD thesis.

AW.2. HiPEAC Paper Award as co-author of the paper - Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Aleksandar Brankovic, Jovana Jovic, Cristina Silvano. "A Correlation-Based Design Space Exploration Methodology for Multi-Processor Systems-on-Chip " DAC - Design Automation Conference, Anheim, CA, USA, 2010

AW.3. ACM Service Award as General Chair of the International Conference on Computing Frontiers, Como Lake - Italy, 2016.

AW.4. HiPEAC Technology Transfer Award 2020 for the technology - "GeoDock: A Fast and Configurable Pocket-Aware Ligand Pose Generator for High-Throughput Molecular Docking".

AW.5. ACM Service Award as General Chair of the ACM International Conference on Computing Frontiers, Catania - Italy (Virtual), 2020

Professional Activities

NATIONAL AND INTERNATIONAL COMMITTEES

- Chair of the panel for the *Academy of Finland* - Call 2018 - Proposal evaluation procedure for research applications in the field of Electronics and Electrical Engineering
- Panel member for the *Academy of Finland*
  - Call 2017 - Proposal evaluation procedure for research applications in the field of Energy-Efficient ICT Systems of the Future
  - Call 2016 - Proposal evaluation procedure for research applications in the field of Electronics and Electrical Engineering
  - Call 2013 - Proposal evaluation procedure for research applications in the field of Electronics and Processor Architectures
  - Call 2012 - Proposal evaluation procedure for research applications in the field of Electronics and Processor Architectures
- Panel member for the *Ministry of Economy and Finance (MEF), AAMS* (Amministrazione Autonoma dei Monopoli di Stato) - 2011 - Selection procedure for granting the right of implementing and managing the telematic networks for Amusement-with-Prize machines (AWP, aka New Slots) and Video Lottery (VLT)
- Panel member for selection procedures at University-level:
  - Member of the panel at Politecnico di Torino for 1 position as RTD-B, Assistant professor with tenure, November – December 2021;
  - Member of the panel at UniCusano for 1 position as RTD-A, Assistant professor without tenure, May – July 2021;
  - Member of the panel at Politecnico di Milano for the evaluation as Assistant professor without tenure for Antonio Miele, December 2020 – January 2021;

  - Member of the panel at Politecnico di Torino for 1 position as RTD-A, Assistant professor without tenure, May – July 2019;
  - Member of several evaluation procedures for research assistant procedures (Assegno di Ricerca) at Politecnico di Milano, Starting from 2008.

- External contribution to international committees:
  - Reviewer for the *Singapore Ministry of Education (MOE)* - Call 2015
  - Reviewer for the *French National Research Agency (ANR)* - Call 2013
  - Participant to the Scientific Panel for the ISCRA (Italian SuperComputing Resource Allocation) initiative at CINECA

- Member of PhD committees:
  - Member of the examination board at ETH-Zurich for Florian Glaser (2022)
  - Member of the examination board at Politecnico di Torino for Mohammadamir Mansoori (2022)
  - Member of the examination board at VSB - Technical University of Ostrava for Vojtech Cima (2021)
  - President of the commission and member of the examination board at Politecnico di Milano for Ahmet Erdem (2020)
  - Member of the examination board at University of Porto for Luis Alexandre Cubal dos Reis (2020)
  - Member of the examination board at University of Turku for Anil Kanduri, acting as external reviewer (2019)
  - President of the commission and member of the examination board at Politecnico di Milano for Emanuele DelSozzo, Davide Gadioli, Giuseppe Natale, Rabozzi Marco, Scolari Alberto (2019)

MEMBERSHIP IN NATIONAL AND INTERNATIONAL SOCIETIES

- Senior Member IEEE - Institute of Electrical and Electronics Engineers
- Member ACM and SIGMICRO - Association for Computing Machinery, Special Interest Group on Microarchitectures
- Member of HiPEAC - European Network on High-performance Embedded Architecture and Compilation
- Member of EuroLab4HPC - European Research Center of Excellence in High Performance Computing Systems

CONTRIBUTION TO NATIONAL AND INTERNATIONAL RESEARCH PROJECTS

- *EuroCC-Italy-PoC - Experiment with the use of Quantum Computing methodologies in the context of new drug design simulations* - Period: 2021-2022
  Role: PoliMi Principal Investigator
  Activities: The project aims to develop a problem-solving approach by selecting the ideal location of the ligand inside a protein pocket through Quantum Annealing (QA) techniques. The project studies the translation of the problem into Higher-order Unconstrained Binary Optimization (HUBO) form, to make it solvable by a quantum annealer, such as the D-Wave machines. The goal is to understand the peculiarities and limitations of these devices and compare their performance with state-of-the-art molecular docking methods.

- *H2020-JTI-EuroHPC-956137-LIGATE - LIgand Generator and portable drug discovery platform AT Exascale* - Period: 2021-2023
  Role: Project Technical Coordinator, PoliMi Principal Investigator and Research Team Member
  Activities: LIGATE project extends the EXSCALATE platform with the primary objective to exploit the potential of supercomputing combined with life science scientific skills in Europe to better and quickly face pandemic situations of supranational interest. In particular, the coordinated PoliMi activities are the following: (i) the optimization and tuning of parallel applications, and in particular the EXSCALATE platform, on novel heterogeneous architectures; (ii) the development of the molecular docking procedure with the integration of Machine Learning techniques always keeping in mind the urgent computing scenario.

- *EITDigital-21479-C2101 - Digital Manufacturing: Development of a new entry point at PoliMi*
  Role: Project Responsible - Period: 2021
  Activities: The project aims at the preparation activities, alignment to other entry/exit universities, and the implementation of the entry-year curriculum (detailed syllabus) for the EITDigital Master on Digital Manufacturing.

- *H2020-ICT-957269-EVEREST - dEsign enVironmEnt foR Extreme-Scale big data analyTics on heterogeneous platforms"* - Period: 2020-2023
  Role: Co-applicant, Innovation Committee Member, Work-Package Leader and Research Team Member
  Activities: The EVEREST project aims at developing a holistic design environment that simplifies the programmability of High Performance Big Data analytics for heterogeneous, distributed, scalable and secure systems. In particular, the activity in charge him includes the exploration and optimization of application parameters and code versions considering a virtualized computing node. Moreover, he is the coordinator of the use case development and evaluation activities.

- *H2020-SC1-PHE-CORONAVIRUS-101003551-EXSCALATE4CoV - EXaSCale smArt pLatform Against paThogEns for Corona Virus"* - Period: 2020-2021
  Role: PoliMi Principal Scientist and Research Team Member
  Activities: Goal of the project is the usage of supercomputers to support the development of novel therapeutic solutions to Covid-19. In particular, the coordinated activity is composed of the porting and continuous optimization of the exascale virtual screening software within the EXSCALATE platform, targeting different European supercomputers and considering the urgent scenario.

- *High Performance Virtual Screening Software Optimization for Urgent Computing (DOMPE'/POLIMI project)* - Period: 2020-2022
  Role: PoliMi Principal Investigator and Research Team Member
  Activities: Design and optimization of a novel geometric docking application for drug discovery in the context of the EXSCALATE (EXaSCale smArt pLatform Against paThogEns - www.exscalate.eu) framework. The activity includes the porting of the software in novel HPC node architectures using GPUs. Autotuning techniques and approximate computing approaches will be adopted and studied for speeding up the computation in the context of Urgent Computing.

- *H2020-FETHPC-671623-ANTAREX: AutoTuning and Adaptivity appRoach for Energy efficient eXascale HPC systems (FET Project)* - Period: 2015-2019
  Role: Co-applicant, Deputy-Coordinator, Task Leader and Research Team Member
  Activities: Development of a self-adaptive application-level framework for energy efficient execution in HPC platforms. The framework exploits autonomous and and approximate computing concepts by tuning application-level knobs according to dynamically changing functional and extra-functional requirements. He was co-applicant of the project.

- *FP7-ICT-611146-CONTREX : Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties (IP Project)* - Period: 2013-2016
  Role: Co-applicant, Task Leader and Research Team Member
  Activities: Design and implementation of (i) a multi-level design space exploration framework for real-time embedded system and (ii) an application-level run-time monitoring framework for the extra functional properties. He was co-applicant of the project.

- *FP7-ICT-248716-2PARMA : PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures (STREP Project)* - Period: 2010-2013
  Role: Co-applicant and Research Team Member
  Activities: Implementation of an application-specific run-time manager to support application adaptation on multi/many-core architectures. He was co-applicant of the project.

- *ARTEMIS-100230-SMECY : Smart Multicore Embedded SYstems* - Period: 2010-2013
  Role: Research Team Member
  Activities: Definition and implementation of design space exploration techniques to statically support the a system-wide run-time resource manager on a many-core architecture (ST-P2012/STHORM).

- *FP7-ICT-247999-COMPLEX : CO-design and power Management in PLatform-based design space Exploration (IP Project)* - Period: 2009-2013
  Role: Co-applicant, Work-Package Leader, Task Leader and Research Team Member
  Activities: Definition and implementation of power-aware methodologies in a model-driven HW/SW co-design flow based on the introduction of an automatic design space exploration engine. He was co-applicant of the project.

- *FP7-ICT-216693-MULTICUBE : MULTI-objective Design Space Exploration of MULTIprocessor SOC Architectures for Embedded MULTImedia Applications (STREP project)* - Period: 2008-2010
  Role: Co-applicant, Work-Package Leader and Deputy Project Coordinator
  Activities: Coordinator of all the project activities regarding the automatic design space exploration (A-DSE) of multiprocessor architectures. Development of an A-DSE tool in terms of design of experiment modules, exploration algorithms and response surface models. He was co-applicant of the project.

- *FP6-IST-035143-hARTES: Holistic Approach to Reconfigurable Real-Time Embedded Systems (IP Project)* - Period: 2006-2010
  Role: Research Team Member
  Activity: Design and analysis of a reconfigurable multiprocessor platform (called *CERBERO*) to internally validate an high-level HW-SW partitioning and mapping tool.

- *Medea+-2A708-LoMoSa: Low Power expertise for Mobile and multi-media System Applications* - Period: 2005-2008
  Role: Co-applicant, Task Leader and Research Team Member (USI-ALARI)
  Activities: Analysis and implementation of low-level security services and power-aware design techniques for the ST-NoC communication architecture. He was co-applicant of the project.

- *Low Power Network on Chip and Multiprocessor Platforms (STMicroelectronics/POLIMI project)* - Period: 2006-2008
  Role: Task Leader and Research Team Member
  Activities: Analysis and optimization of the synchronization problem in NoC-based multiprocessors. Definition of power-aware policies for the on-chip interconnection.

- *MIUR FIRB MAIS: Multichannel Adaptive Information Systems* - Period 2002-2006
  Role: Research Team Member

Activities: Design and implementation of power estimation (SW oriented) and optimization techniques (architecture-oriented) for the low-power LX-VLIW architectures designed by STMicroelectronics.

- *Low Power Network on Chip and Embedded Architectures (STM/POLIMI project)* - Period: 2003-2005
  Role: Research Team Member
  Activities: Design and Implementation of an on-chip interconnection architecture for embedded systems based on a pure NoC philosophy. Analysis of the NoC-based Hyperprocessor architecture designed by STMicroelectronics from a power/performance/programmability point of view.

- *Medea+-A207 - Silicon Application Platform for Pocket Multimedia* - Period: 2002-2005
  Role: Research Team Member (STMicroelectronics)
  Activities: Design and implementation of power estimation techniques for the ST-BUS architecture based on gate level analysis.

RESOURCE ALLOCATION PROJECTS SUBJECT TO PEER-REVIEW

- *EHPC-DEV-2021D02-049 (EuroHPC Development Access): Automated Workflow for Computer Accelerated Drug Discovery on Exascale Machines - Period: 02.2022-02.2023*
  Role: Principal Investigator
  Resources: 1.920.000 CPU core hours, 384.000 GPU core hours
  Activities: This project aims to automate the drug design process by minimizing the human effort required in the different phases of the process, including input parameters preparation, the management of data sets with billions of molecules, and the interaction with queue manager to handle jobs.

- *CINECA-ISCRA-C - Quantum Annealing for Small Molecule Unfolding* - Period: 2021–2022
  Role: Principal Investigator
  Resources: 16K core hours, 3 QPU hours.
  Activities: The project explores the possibility to use the D-WAVE quantum annealer to optimize a specific phase of the molecular docking procedure called Small Molecule Unfolding, SMU.

- *LEXIS-COVID-Computation (First Stage) - Using HPCaaS for Virtual Screening* - Period: 2021-2022
  Role: Principal Investigator
  Resources: 750K core hours
  Activities: The project adopts an HPC as a service middleware to support a virtual screening approach under an urgent computing scenario.

- *IT4INNOVATION-DD-Project - HPCaaS for COVID Computation* - Period: 2020-2021
  Role: Co-Principal Investigator (with Jan Martinovich IT4Innovation)
  Resources: 200K core hours
  Activities: The project explores the possibility to use an HPC as a service middleware to support a recommender system based virtual screening approach in the COVID-19 context.

TECHNOLOGY TRANSFER

- GeoDock - Fast and Configurable Pocket-Aware Ligand Pose Generator for High-Throughput Molecular Docking - Technology transferred to DOMPE' Farmaceutici (HiPEAC Technology Transfer Award 2020) - Type: Software

- LigenHT - High-Throughput implementation of the LIGEN platform for the virtual screening task capable to run up to an entire supercomputing center - Technolgy transferred to DOMPE' Farmaceutici within the context of the Exscalate4Covid Project - Type: Software

- APTDR - Adaptive Probabilistic Time Dependent Routing Algorithm for an efficient arrival time estimation - Technology transferred to IT4Innovation (Czech Supercomputing Center) - Type: Software
- STNoC-OCCN - STNoC Performance and Power Model using OCCN - Technology transferred to STMicroelectronics - Type: Software/Simulation Model
- DPU/NSM - Data Protection Unit and Network Security Manager for Networks-on-Chip - Technology transferred to STMicroelectronics (Patents PA.1 and PA.2) - Type: Hardware Design
- Additional technologies have been transferred to industries and research centers within the context of European Projects.

CONFERENCE AND WORKSHOP ORGANIZATION

Program Chair

- ReC4P - International Workshop on Reconfigurable Computing for HPC and HPDA - (2015)
- RAPIDO - International Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools - (2013 – 2017, 2019)

Steering Committees

- CF - International Conference on Computing Frontiers (2016 - Now)
  - *Deputy chair* (2022 - Now)
- RAPIDO - International Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (2022 - Now)

Organizing Committees

- CF - International Conference on Computing Frontiers - *General Chair* (2016, 2020), *Registration Chair* (2017), *Workshop Chair* (2019), *Poster Chair* (2022)
- ANDARE - Workshop on AutotuniNg and aDaptivity AppRoaches for Energy efficient HPC Systems - Co-located with PACT - *Publicity Chair* (2017, 2018)
- ReC4P - International Workshop on Reconfigurable Computing for HPC and HPDA - *Organizing Committee* (2015)
- RAPIDO - International Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools - *Organizing Committee* (2013 – 2022)
- ARCS - International Conference on Architecture of Computing Systems - *Publicity Chair and Local Committee* (2011)
- MICRO - International Symposium on Microarchitecture - *Local Arrangements Chair* (2008)

Track/Topic Chair

- DATE - Design Automation and Test in Europe - *Topic Chair on System Specification and Modeling* - 2022
- DATE - Design Automation and Test in Europe - *Topic Co-Chair on System Specification and Modeling* - 2020 and 2021

- CODES+ISSS - International Conference on Hardware/Software Codesign and System Synthesis - *Track Chair on System Level Design* - 2017
- EUC - International Conference on Embedded and Ubiquitous Computing - *Track Chair on Power Efficient Computing* - 2014
- PARMA - International Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures - *Track Chair on Design Space Exploration and Many-core Architecture Customization* - 2010, 2011

Program Committee Membership

- DATE (2006 – 2010, 2015 – 2022) - Design Automation and Test in Europe.
  - In 2017 and 2019 member of the special committee for the *Best Interactive Presentation Award*.
  - In 2022 member of the special committee for the *Best Paper Award selection*, D-track.
- CF (2012, 2015, 2017–2019, 2022) - International Conference on Computing Frontiers
  - In 2017, 2019, 2022 member of the committee for the *Best Paper Award*.
  - In 2019, 2022 member of the committee for the *Best Poster Award*.
- HiPC (2021, 2022) - IEEE International Conference on High Performance Computing, Data, and Analytics
- MCSoC (2014 – 2022) - International Symposium on Embedded Multicore/Many-core Systems-on-Chip
- RAPIDO (2011 – 2022) - International Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools
- CODES+ISSS (2017–2021) - International Conference on Hardware/Software Codesign and System Synthesis
- ReConFig (2016–2019) - International Conference on ReConFigurable Computing and FPGAs
- FPL (2015 – 2020) - International Conference on Field-Programmable Logic and Applications
- ASAP (2018) - International Conference on Application-specific Systems, Architectures and Processors
- IC-SAMOS (2015 – 2022) - International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
- EUC (2005, 2014 – 2015) - International Conference on Embedded and Ubiquitous Computing
- IA^3 (2011 – 2017) - International Workshop on Irregular Applications: Architectures and Algorithms
- CS^2 (2014, 2015) - International Workshop Cryptography and Security in Computing Systems
- MOMAC (2014 – 2016) - International Workshop on Multi-Objective MAny-Core design
- MES (2013 – 2017) - International Workshop on Many-core Embedded Systems
- WRC (2013 – 2017) - International Workshop on Reconfigurable Computing
- PARMA-DITAM (2014 – 2018) - Joint International Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures and on Design Tools and Architectures for Multi-Core Embedded Computing Platforms

- OPTIM (2016–2019) - International Workshop on Optimization Issues in Energy Efficient HPC & Distributed Systems
- ANDARE (2017–2018) - Workshop on AutotuniNg and aDaptivity AppRoaches for Energy efficient HPC Systems
- NoCArc (2008 – 2016) - International Workshop on Network on Chip Architectures
- AASC (2015) - International Workshop on Architecture-Aware Simulation and Computing
- PARMA (2010 – 2013) - International Workshop on Parallel Programming and Run-Time Management Techniques for Many-core Architectures
- SOC (2012) - International Symposium on System-on-Chip
- CDES (2007) - International Conference on Computer Design
- ESA (2007) - International Conference on Embedded Systems and Applications

Conferences and Workshops as external reviewer or sub-reviewer (not in the TPC)

- DAC - Design Automation Conference, MICRO - International Symposium on Microarchitecture, ARCS - International Conference on Architecture of Computing Systems, DATE - Design Automation and Test in Europe, ICCAD - International Conference on Computer Aided Design, PATMOS - International Workshop on Power and Timing Modelling, SAC - Symposium on Applied Computing, EUC - Embedded and Ubiquitous Computing, SAMOS - International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, FPL - International Conference on Field Programmable Logic and Applications, VLSI-SoC - IFIP/IEEE International Conference on Very Large Scale Integration, International Symposium on System-on-Chip, ACM International Conference on Computing Frontier, ACM/IEEE International Symposium on Networks-on-Chip, IEEE Symposium on Application Specific Processors (SASP), HiPEAC - International conference on High-Performance Embedded Architectures and Compilers, ICPP - International Conference on Parallel Processing, ISCAS - International Symposium on Circuits and Systems.

SERVICES IN JOURNALS AND CONFERENCES

Editorial Board Member

- Journal of System Architecture - Elsevier - ISSN: 1383-7621 - CiteScore: 7.2 - Impact Factor: 5.836 - Scimago Journal Ranking: Q1 (Hardware and Architecture) - Period: 2019 - Now
- Electronics, Computer Science and Engineering section - Mdpi - ISSN: 2079-9292 - CiteScore: 3.7 - Impact Factor: 2.69 - Scimago Journal Ranking: Q2 (Hardware & Architecture) - Period: 2020 - Now

Guest Editor

- International Journal of Parallel Programming - Springer - *Special Issue on Computing Frontiers*. - ISSN: 0885-7458 / 1573-7640 - CiteScore: 1.55 - Impact Factor: 1.258 - SCImago Journal Ranking: Q3 (Software) - Period: 2016 - 2018.

Reviewer

- IEEE Transactions on Computers (TC), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Very Large Scale Integration Systems (TVLSI), ACM Transactions on Embedded Computing Systems (TECS), ACM Transactions on Design Automation of Electronic Systems (TODAES), ACM Transactions on Architecture and Code Optimization (TACO), IEEE Transactions on Cybernetics (TCYB), IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE Computer Architecture Letters (CAL), IEEE Transactions on Multi-Scale Computing Systems (TMSCS), ELSEVIER Microprocessors and Microsystems: Embedded Hardware Design (MICPRO), ELSEVIER Journal of System Architecture (JSA), ELSEVIER Computers & Electrical Engineering (COMPELECENG), SPRINGER Design Automation for Embedded Systems (DAES), SPRINGER Optimization Letters (OL), SPRINGER Journal of Supercomputing (JSUPE), IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), IEEE Embedded Systems Letters (ESL), IET Computers & Digital Techniques (IET-CDT), SPRINGER Journal of Computer Science and Technology (JCST), MDPI - Journal of Low Power Electronics and Applications (JLPEA), ELSEVIER Simulation Modelling Practice and Theory (SIMPAT), ELSEVIER The Journal of Systems & Software (JSSoftware).

INSTITUTIONAL ROLES AND RESPONSIBILITIES AT POLITECNICO DI MILANO

- Politecnico di Milano representative within the EIT-Digital association - European Institute of Innovation and Technology - for the period 2020 – 2022.
- Member of the Tutoring Committee for the School of Industrial and Information Engineering at Politecnico di Milano (AY 14/15 – 18/19)
- Member of the Scientific Committee for the Computer Science and Engineering Track within the Honours Programme *Scientific Research in Information Technology* (AY 18/19 – Now)
- Member of the *Offices & Working Spaces* commission for the Computer Science and Engineering section of the Dept. of Electronics, Information, and Bioengineering at Politecnico di Milano (2019 – Now)
- Responsible for the foreign students within the Computer Science and Engineering track (graduate level) at Politecnico di Milano (AY. 08/09 – Now)
  Tasks: Welcome Day organization, tutors supervision, and study plan pre-assessment

Talks and Tutorials

INVITED TALKS

- "Mapping and Topology Customization Approaches for Application-Specific STNoC Designs" at EPFL in 2007
- "Data Parallel Application Adaptivity and System-Wide Resource Management in Many-Core Architectures" at the *International Symposium on Applied Reconfigurable Computing*, 2014
- "Autotuning and adaptivity in energy efficient HPC systems: The ANTAREX toolbox" at the *ACM International Conference on Computing Frontiers*, 2018
- "Autotuning and adaptivity in energy efficient exascale HPC systems" at the *HPCAFE-2017: High-Performance Computing Approaches for Monitoring, Exploring, Optimizing and Autotuning* (European HPC Summit Week), 2017

- "Energy Efficient Computing Systems Exploiting Online Tuning and Output Quality Management" at the *CPS Summer School - Designing Cyber-Physical Systems From concepts to implementation*, 2018
- "Autotuning and Adaptivity Approaches for Energy Efficient HPC Systems: The ANTAREX Toolbox" at the PRACE On Demand Training Event/School on *Monitoring, Compilation and Autotuning Approach for Energy-Efficient HPC Systems*, 2018
- "An Introduction to Dynamic Autotuning" at the PRACE On Demand Training Event/School on *Monitoring, Compilation and Autotuning Approach for Energy-Efficient HPC Systems*, 2018
- "Dynamic Application Autotuning for Approximate Computing" at the *NIPS Summer School - Architectures and Algorithms for Energy-Efficient IoT and HPC Applications*, 2019
- "Exscalate4CoV: Towards an exascale-ready docking platform targeting urgent computing" at the *CECAM Seminars - The importance of being H.P.C. Earnest*, 2020
- "Tuning an Exascale-Ready Drug-Discovery Platform Targeting Urgent Computing for COVID-19" at the *ESTECO User Meeting Conference*, 2020.
- "Molecule Unfolding using Quantum Anneling" at the *DWAVE Webinar Series*, 2021, with K. Mato, R. Mengoni, D. Ottaviani.
- "Climbing EVEREST: dEsign enVironmEnt foR Extreme-Scale big data analyTics on heterogeneous platforms", at *DATE Workshop on Data-driven applications for industrial and societal challenges: Problems, methods, and computing platforms* 2022.
- "EXSCALATE: An Extreme-Scale Virtual Screening Platform for Drug Discovery Targeting Polypharmacology to Fight SARS-CoV-2", at the *International Conference on High Performance Computing & Applications*, 2022.

PANELS

- Member of the panel "Designing Cyber-Physical Systems: Incremental Approaches or Disruptive Technologies?" at the ACM International Conference on Computing Frontiers, 2017
- Member of the panel "Power consumption in DataCenters, HPC and AI workloads" at the on-line Webinar on Energy reduction for AI workloads: New solutions from ANDREAS and AI-SPRINT, 2021.

TUTORIALS

- "CONTREX: Virtual Integration Testing for Mixed-Criticality Systems under Consideration of Power and Temperature Constraints" at the *HiPEAC Conference - High Performance and Embedded Architecture and Compilation*, 2016.
- "Runtime Autotuning: the mArgot approach" at the *PRACE On Demand Training Event/School on Monitoring, Compilation and Autotuning Approach for Energy-Efficient HPC Systems*, 2018
- "Runtime Autotuning: the mArgot approach" within the "The ANTAREX Approach to Adaptively Optimize and Enforce Extra-Functional Properties on HPC Applications" tutorial at the International Conference on Parallel Architectures and Compilation Techniques - PACT18.

Teaching Activities

COURSE RESPONSIBILITY

- Computing Infrastructure - (5 credits)
  Politecnico di Milano - Computer Science and Engineering - Graduate level
  Bocconi University/Politecnico di Milano - Cyber Risk Strategy and Governance - Graduate level
  Academic Year: 20/21, 21/22
- Impianti e Servizi Informatici - (10 credits)
  Politecnico di Milano - Computer Engineering, Online Program - Undergraduate level
  Academic Years: 21/22
- Reti Logiche - (5 credits)
  Politecnico di Milano - Computer Engineering - Undergraduate level
  Academic Years: 15/16, 16/17, 17/18, 18/19, 19/20, 20/21, 21/22
- Prova Finale (Progetto di Reti Logiche) - (1 credit)
  Politecnico di Milano - Computer Engineering - Undergraduate level
  Academic Years: 17/18, 18/19, 19/20, 20/21, 21/22
- Energy Efficienct and Approximate Computing
  Politecnico di Milano - PhD in Information Technology - PhD level
  Academic Year: 20/21
- Progetto di Ingegneria Informatica / GeoInformatic project - (5 credits)
  Politecnico di Milano - Computer Science and Engineering - Undergraduate level
  Politecnico di Milano - GeoInformatic Engineering - Graduate level
  Academic Year: 20/21
- Computing Systems - (10 credits)
  Politecnico di Milano - Engineering Physics - Graduate level
  Academic Years: 18/19, 18/19, 19/20
- Computing Systems for Engineering Physics - (10 credits)
  Politecnico di Milano - Engineering Physics - Graduate level
  Academic Years: 15/16, 16/17, 17/18, 18/19
- Informatica ed Elementi di Informatica Medica [1] (7 credits)
  Politecnico di Milano - Biomedical Engineering - Undergraduate level
  Academic Years: 09/10, 10/11, 11/12, 12/13, 13/14, 14/15
- Informatica B - Informatica per Applicazioni Scientifiche e Industriali (10 credits)
  Politecnico di Milano - Engineering Physics - Graduate level
  Academic Years: 12/13, 13/14, 14/15
- Metodologie di Progetto Hardware/Software (5 credits)
  Politecnico di Milano - Computer Engineering - Graduate level
  Academic Year: 09/10
- Sistemi Informatici (7 credits)
  Politecnico di Milano - Automation Engineering - Undergraduate level
  Academic Year: 08/09

- Cultura Tecnologica di Progetto - Informatica (2.5 credits)
  Politecnico di Milano - Product Design - Undergraduate level
  Academic Year: 07/08

- Design Laboratory 2 (3 credits)
  ALaRI - Universita' della Svizzera Italiana - Embedded System Design - Graduate level
  Academic Years: 05/06, 06/07, 07/08

- Progettazione VLSI per il consumo di potenza, l'area e le prestazioni
  Politecnico di Milano - Information Technology PhD - PhD level
  Academic Year: 06/07

TEACHING ASSISTANT

- Computing Infrastructure (20h)
  Politecnico di Milano - Computer Science and Engineering - Graduate level
  Course Responsible: Prof. Manuel Roveri
  Academic Year: 19/20

- Advanced Algorithms and Parallel Programming (10h)
  Politecnico di Milano - Computer Science and Engineering - Graduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Year: 19/20

- Informatica ed Elementi di Informatica Medica [1] (24h)
  Politecnico di Milano - Biomedical Engineering - Undergraduate level
  Course Responsible: Prof. Manuel Roveri
  Academic Years: 15-16, 16-17, 17-18, 18-19

- Reti Logiche A (20h)
  Politecnico di Milano - Computer Science and Engineering - Undergraduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Years: 10-11, 09-10, 08-09, 07-08, 06-07, 05-06, 04-05, 03-04

- Reti Logiche B (20h)
  Politecnico di Milano - Electronic Engineering - Undergraduate level
  Course Responsible: Prof. Fabrizio Ferrandi and Prof. Mariagiovanna Sami
  Academic Years: 08-09, 07-08, 06-07, 05-06, 04-05, 03-04

- Metodologie di Progetto Hardware e Laboratorio (20h)
  Politecnico di Milano - Computer Science and Engineering - Graduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Years: 07-08, 06-07, 05-06, 04-05

- Metodologie di Progetto Hardware (10h)
  Politecnico di Milano - Computer Science and Engineering - Graduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Year: 03-04

- Laboratorio di Metodologie di Progetto Hardware (10h)
  Politecnico di Milano - Computer Science and Engineering - Graduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Year: 03-04

- Calcolatori Elettronici A (20h)
  Politecnico di Milano - Computer Science and Engineering - Undergraduate level
  Course Responsible: Prof. Fabrizio Ferrandi
  Academic Year: 02-03

- Calcolatori Elettronici (40h)
  Politecnico di Milano - Electronic and Telecommunication Engineering - Graduate
  Course Responsible: Prof. Cristina Silvano
  Academic Years: 02-03, 01-02

OTHER TEACHING ACTIVITIES

- Coding (30h)
  Politecnico di Milano - TechCamp - High-school level
  Period: Summer 2019, Summer 2021, Summer 2022.

- Coding Base Edition (30h)
  Liceo Scientifico "Donatelli-Pascal", Milano - PON "Life Design" - High-school level
  Period: Spring 2019

- Coding Advanced Edition (30h)
  Liceo Scientifico "Donatelli-Pascal", Milano - PON "Life Design" - High-school level
  Period: Spring 2019

STUDENTS' SUPERVISION

PhD Students Supervision

- *Marco Ceriani - Advisor*, 2010–2014
  Title: "Design Methodologies and Multiprocessor Architectures for Irregular HPC Applications"

- *Ioannis Stamelakos - Co-Advisor*, 2012 – 2016
  Title: "Technology-Aware Many-core Architecture Design"

- *Amir H. Ashouri - Co-Advisor*, 2012 – 2016
  Title: "Compiler Auto-Tuning for Embedded Computing Platforms"

- *Davide Gadioli - Advisor*, 2014 – 2019
  Title: "Dynamic Application AutoTuning for Self-Aware Approximate Computing"

- *Emanuele Vitali- Advisor*, 2017 – 2020
  Title: "Mixed Design-time/Run-time Approaches to Application AutoTuning in Heterogeneous Architectures"

- *Roberto Rocco - Advisor*, 2021 – Present
  Title: "Run-Time Self-Adaptive Applications for Efficient Processing in the Computing Continuum"

Graduate Students Supervision

- He advised and co-advised more than 50 students within Politecnico di Milano, ALaRI - USI and STMicrolectronics facilities.

Publication List

PATENTS

PA.1. Valerio Catalano, Riccardo Locatelli, Marcello Coppola, Gianluca Palermo, Leandro Fiorin, Cristina Silvano, "Programmable Data Protection Device, Secure Programming Manager System and Process For Controlling Access to an Interconnect Network for an Integrated Circuit". US Patent Office publication number: US2009089861 (B2).

PA.2. Valerio Catalano, Riccardo Locatelli, Marcello Coppola, Gianluca Palermo, Leandro Fiorin, Cristina Silvano, "Programmable Data Protection Device, Secure Programming Manager System and Process For Controlling Access to an Interconnect Network for an Integrated Circuit". European Patent Office publication number: EP2043324 (A1).

REFEREED INTERNATIONAL JOURNALS

JR.1. Davide Gadioli, Emanuele Vitali, Federico Ficarelli, Chiara Latini, Candida Manelfi, Carmine Talarico, Cristina Silvano, Carlo Cavazzoni, Gianluca Palermo, Gianluca and Andrea R. Beccari. "EXSCALATE: An Extreme-Scale Virtual Screening Platform for Drug Discovery Targeting Polypharmacology to Fight SARS-CoV-2". *IEEE Transactions on Emerging Topics in Computing*. Volume XX, no. YY.
DOI: https://dx.doi.org/10.1109/TETC.2022.3187134

JR.2. Kevin Mato, Riccardo Mengoni, Daniele Ottaviani, and Gianluca Palermo. "Quantum Molecular Unfolding". *Quantum Science and Technology*. Volume 7, no. 3.
DOI: https://dx.doi.org/10.1088/2058-9565/ac73af

JR.3. Pedro Pinto, Joao Bispo, Joao Cardoso, Jorge Gomes Barbosa, Davide Gadioli, Gianluca Palermo, Jan Martinovic, Katerina Slaninova, Cristina Silvano "PEGASUS: Performance Engineering for Software Applications Targeting HPC Systems". *IEEE Transactions on Software Engineering*. Vol. 48, no. 3, pp. 732-754, 1 March 2022,
DOI: https://doi.org/10.1109/TSE.2020.3001257.

JR.4. Mattia Tibaldi, Gianluca Palermo, and Christian Pilato. "Dynamically-Tunable Dataflow Architectures Based on Markov Queuing Models". *Electronics*. Volume 11, no. 4: 555. 2022.
DOI: https://doi.org/10.3390/electronics11040555

JR.5. Murugan, Natarajan A., Artur Podobas, Davide Gadioli, Emanuele Vitali, Gianluca Palermo, and Stefano Markidis. "A Review on Parallel Virtual Screening Softwares for High-Performance Computers". *Pharmaceuticals*. Volume 15, no. 1: 63. 2022.
DOI: https://doi.org/10.3390/ph15010063

JR.6. Roberto Rocco, Davide Gadioli, Gianluca Palermo. "Legio: fault resiliency for embarrassingly parallel MPI applications". *The Journal of Supercomputing*. Volume 78, Issue 4, pp 21752195. 2022.
DOI: https://doi.org/10.1007/s11227-021-03951-w

JR.7. Davide Gadioli, Gianluca Palermo, Stefano Cherubin, Emanuele Vitali, Giovanni Agosta, Candida Manelfi, Andrea R. Beccari, Carlo Cavazzoni, Nico Sanna, Cristina Silvano. "Tunable approximations to control time-to-solution in an HPC molecular docking Mini-App". *The Journal of Supercomputing*. Volume 77, Issue 1, pp 841869. Jan 2021.
DOI: https://doi.org/10.1007/s11227-020-03295-x

JR.8. Emanuele Vitali, Davide Gadioli, Gianluca Palermo, Martin Golasowski, Joo Bispo, Pedro Pinto, Jan Martinovic, Katerina Slaninov, Joo M. P. Cardoso, Cristina Silvano "An Efficient Monte Carlo-based Probabilistic Time-Dependent Routing Calculation Targeting a Server-Side Car Navigation System". *IEEE Transactions on Emerging Topics in Computing*. Volume 9, no. 2, pp. 1006–1019, 2021.
DOI: https://doi.org/10.1109/TETC.2019.2919801

JR.9. Leonardo Arcari, Marco Gribaudo, Gianluca Palermo, Giuseppe Serazzi. "Performance-Driven Analysis for an Adaptive Car-Navigation Service on HPC Systems". *Springer Nature Computer Science*. Volume 1, article 41 (2020).
DOI: https://doi.org/10.1007/s42979-019-0035-7

JR.10. Emanuele Vitali, Davide Gadioli, Gianluca Palermo, Andrea Beccari, Carlo Cavazzoni, Cristina Silvano. "Exploiting OpenMP and OpenACC to accelerate a geometric approach to molecular docking in heterogeneous HPC nodes". *The Journal of Supercomputing*. Volume 75, Issue 7, pp 33743396. July 2019.
DOI: https://doi.org/10.1007/s11227-019-02875-w

JR.11. Cristina Silvano, Giovanni Agosta, Andrea Bartolini, Andrea R. Beccari, Luca Benini, Loc Besnard, Joo Bispo, Radim Cmar, Joo M. P. Cardoso, Carlo Cavazzoni, Daniele Cesarini, Stefano Cherubin, Federico Ficarelli, Davide Gadioli, Martin Golasowski, Antonio Libri, Jan Martinovic, Gianluca Palermo, Emanuele Vitali. "The ANTAREX domain specific language for high performance computing". Microprocessors and Microsystems Embedded Hardware Design. Volume 68: Pages 58-73. July 2019.
DOI: https://doi.org/10.1016/j.micpro.2019.05.005

JR.12. Stamelakos Ioannis, Xydis Sotirios, Palermo Gianluca, Silvano Cristina. "Workload- and Process-Variation Aware Voltage/Frequency Tuning for Energy Efficient Performance Sustainability of NTC Manycores". *Integration, the VLSI Journal*. Volume 65, Pages 252-262, March 2019.
DOI: https://doi.org/10.1016/j.vlsi.2018.02.013

JR.13. Davide Gadioli, Emanuele Vitali, Gianluca Palermo, Cristina Silvano: mARGOt: A Dynamic Autotuning Framework for Self-Aware Approximate Computing. *IEEE Transactions on Computers*. Volume 68 Issue 5, pp. 713-728, 2019.
DOI: https://doi.org/10.1109/TC.2018.2883597

JR.14. Amir H. Ashouri, William Killian, John Cavazos, Gianluca Palermo, Cristina Silvano. "A Survey on Compiler Autotuning using Machine Learning" *ACM Computing Surveys*. Volume 51, Issue 5. pp 96:1-96:42. 2019
DOI: https://doi.org/10.1145/3197978

JR.15. Amir H. Ashouri, Andrea Bignoli, Gianluca Palermo, Cristina Silvano, Sameer Kulkarni, and John Cavazos. "MiCOMP: Mitigating the Compiler Phase-Ordering Problem Using Optimization Sub-Sequences and Machine Learning". *ACM Transactions on Architecture and Code Optimization*. Volume 14, Issue 3, Article 29 (September 2017), 28 pages.
DOI: https://doi.org/10.1145/3124452

JR.16. Marco Ceriani, Simone Secchi, Oreste Villa, Antonino Tumeo, Gianluca Palermo. "Exploring Efficient Hardware Support for Applications with Irregular Memory Patterns on Multinode Manycore Architectures", *IEEE Transactions on Parallel and Distributed Systems*. Volume 28, Issue 6 (June 2017), 1635-1648.
DOI: https://doi.org/10.1109/TPDS.2014.2345073

JR.17. Gruttner Kim, Gorgen Ralph, Schreiner Sren, Herrera Fernando, Penil Pablo, Medina Julio, Villar Eugenio, Palermo Gianluca, Fornaciari William, Brandolese Carlo, Gadioli Davide, Vitali Emanuele, Bocchio Sara, Ceva Luca, Azzoni Paolo, Poncino Massimo, Vinco Sara, Macii Enrico, Cusenza Salvatore, Favaro John, Valencia Raul, Sander Ingo, Rosvall Kathrin, Khalilzad Nima, Quaglia Davide. "CONTREX: Design of embedded mixed-criticality CONTRol systems under consideration of EXtra-functional properties". *Microprocessors and Microsystems* Vol. 51, 2017. pp. 39–55, ISSN: 0141-9331. DOI: 10.1016/j.micpro.2017.03.012

JR.18. Amir Hossein Ashouri, Giovanni Mariani, Gianluca Palermo, Eunjung Park, John Cavazos, and Cristina Silvano. "COBAYN: Compiler Autotuning Framework using Bayesian Networks". *ACM Transactions on Architecture and Code Optimization*. Volume 13, Issue 2, Article 21 (June 2016), 25 pages.
DOI: http://dx.doi.org/10.1145/2928270

JR.19. Parinaz Sayyah, Mihai T. Lazarescu, Sara Bocchio, Gianluca Palermo, Davide Quaglia, Alberto Rosti, Luciano Lavagno. "Virtual Platform-based Design Space Exploration of Power-Efficient Distributed Embedded Applications", *ACM Transactions on Embedded Computing Systems*. Volume 14 Issue 3, Article 49, May 2015.

JR.20. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "DESPERATE++: An Enhanced Design Space Exploration Framework using Predictive Simulation Scheduling", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Volume 34, no. 2, pp. 293-306, Feb. 2015.

JR.21. Sotirios Xydis, Gianluca Palermo, Vittorio Zaccaria, Cristina Silvano. "SPIRIT: Spectral-Aware Pareto Iterative Refinement Optimization for Supervised High Level Synthesis", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Volume 34, no. 1, pp. 155-159, Jan. 2015.

JR.22. Leandro Fiorin, Gianluca Palermo and Cristina Silvano. "A Configurable Monitoring Infrastructure for NoC-based Architectures", *IEEE Transactions on VLSI Systems*. vol. 22, no. 11, pp. 2438-2442, Nov. 2014.

JR.23. Fernando Herrera, Hector Posadas, Pablo Penil, Eugenio Villar, Francisco Ferrero, Raul Valencia and Gianluca Palermo. "The COMPLEX Methodology for UML/MARTE Modelling and Design Space Exploration of Embedded Systems" *Elsevier - Journal of System Architectures*, Volume 60, Issue 1 (January 2014), 55-78.

JR.24. Kim Gruttner, Philipp A. Hartmann, Kai Hylla, Sven Rosinger, Wolfgang Nebel, Fernando Herrera, Eugenio Villar, Carlo Brandolese, William Fornaciari, Gianluca Palermo, Chantal Ykman-Couvreur, Davide Quaglia, Francisco Ferrero, Raul Valencia. "The COMPLEX reference framework for HW/SW Co-Design and Power Management Supporting Platform-Based Design-Space Exploration" *Elsevier Journal - Microprocessors and Microsystems: Embedded Hardware Design*. Volume 37, Issue 8, Part C, November 2013, Pages 966–980.

JR.25. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria and Cristina Silvano. "Design Space Exploration and Run-time Resource Management for Multi-cores", *ACM Transactions on Embedded Computing Systems*. Volume 13 Issue 2, September 2013, Article No. 20.

JR.26. Giovanni Mariani, Gianluca Palermo, Vittorio Zaccaria and Cristina Silvano. "ARTE: an Application-specific Run-Time Management Framework for Multi-cores based on Queuing Models", *Elsevier Journal - Parallel Computing*, Volume 39 (2013), pp. 504-519.

JR.27. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "A Variability-Aware Robust Design Space Exploration Methodology for CMPs", *ACM Transactions on Embedded Computing Systems*. Volume 11, Issue 2, July 2012, pp. 29.1-29.28.

JR.28. Giovanni Mariani, Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "OSCAR: an Optimization Methodology Exploiting Spatial Correlation in Multi-core Design Spaces", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Volume 21 Issue 5, May 2012, pp. 740-753.

JR.29. Chantal Ykman-Couvreur, Prabhat Avasare, Giovanni Mariani, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "Linking run-time resource management of embedded multi-core platforms with automated design-time exploration", *IET Computers and Digital Techniques*. Vol. 5. Issue 2, 2011, pp. 123-135.

JR.30. Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria. "ReSPIR: A Response Surface-based Pareto Iterative Refinement for Application-Specific Design Space Exploration", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*. Volume 28 Issue 12, December 2009 pp. 1816-1829.

JR.31. Christian Pilato, Antonino Tumeo, Gianluca Palermo, Fabrizio Ferrandi, PierLuca Lanzi and Donatella Sciuto. "Improving Evolutionary Exploration to Area-Time Optimization of FPGA Designs", *Journal of System Architectures, Elsevier*. Volume 54, Issue 11, November 2008, Pages 1046-1057

JR.32. Leandro Fiorin, Gianluca Palermo, Cristina Silvano and Valerio Catalano. "Secure Memory Accesses on Network-on-Chip", *IEEE Transactions on Computers*. Volume 57 Issue 9, September 2008 pp. 1216-1229.

JR.33. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "Exploration of Distributed Shared Memory Architectures for NoC-based Multiprocessors", *Journal of System Architectures, Elsevier*. Volume 53, Issue 10, October 2007 pp. 719-732.

JR.34. Giovanni Agosta, Gianluca Palermo, Cristina Silvano. "Efficient Architecture/Compiler Co-Exploration Using Analytical Models", *Design Automation for Embedded Systems*, Springer, Volume 11, Issue 1, March 2007, pp. 1-23.

JR.35. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "Efficient Synchronization for Embedded on-Chip Multiprocessors", *IEEE Transactions on VLSI Systems*. Volume 14 Issue 10, October 2006 pp. 1049-1062.

JR.36. Matteo Monchiero, Gianluca Palermo, Cristina Silvano, Oreste Villa. "An Efficient Synchronization Technique for Multiprocessor Systems on-Chip", *ACM SIGARCH Computer Architecture News*, Volume 34 , Issue 1 (March 2006) pp. 33-40.

JR.37. Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria. "Multi-Objective Design Space Exploration of Embedded Systems", *Journal of Embedded Computing*. IOS Press, 1(3) Month(January), 2006, pp. 305-316.

JR.38. Matteo Monchiero, Gianluca Palermo, Mariagiovanna Sami, Cristina Silvano, Vittorio Zaccaria, Roberto Zafalon. "Low-Power Branch Prediction Techniques for VLIW Architectures: A Compiler-Hints Based Approach", *Integration, the VLSI Journal*. Elsevier. 38(3) Month(January), 2005, pp. 515-524.

EDITORIAL CONTRIBUTIONS

ED.1. Antonino Tumeo, Hubertus Franke, Gianluca Palermo, John Feo: Guest Editorial: Special Issue on Computing Frontiers. International Journal of Parallel Programming 46(2): 333-335 (2018)

ED.2. Gianluca Palermo, John Feo, Antonino Tumeo, Hubertus Franke: Proceedings of the ACM International Conference on Computing Frontiers, CF'16, Como, Italy, May 16-19, 2016. ACM 2016, ISBN 978-1-4503-4128-8

ED.3. Gianluca Palermo, Daniel Gracia Perez, Morteza Biglari-Abhari, Daniel Chillet, Smal Niar, Adam Morawiec: Proceedings of the 2015 Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, RAPIDO@HiPEAC 2015, 21 January, 2015, Amsterdam, The Netherlands. ACM 2015, ISBN 978-1-60558-699-1

ED.4. Daniel Gracia Perez, Morteza Biglari-Abhari, Daniel Chillet, Gianluca Palermo: Proceedings of the 2014 Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, RAPIDO '14, 22 January, 2014, Vienna, Austria. ACM 2014, ISBN 978-1-4503-2471-7

ED.5. Daniel Gracia Perez, Morteza Biglari-Abhari, Daniel Chillet, Gianluca Palermo: Proceedings of the 2013 Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools, RAPIDO '13, 21 January, 2013, Berlin, Germany. ACM 2012, ISBN 978-1-4503-1539-5

ED.6. Cristina Silvano, Marcello Lajolo, Gianluca Palermo (Eds.) "Low Power Networks-on-Chip" SPRINGER, 1st Edition., 2011, ISBN: 978-1-4419-6910-1

INTERNATIONAL BOOKS AND BOOK CHAPTERS

BC.1. Amir H. Ashouri, Gianluca Palermo, John Cavazos, Cristina Silvano. "Automatic Tuning of Compilers Using Machine Learning". SpringerBriefs in Applied Sciences and Technology, Springer 2018, ISBN 978-3-319-71488-2, pp. 1-118

BC.2. Cristina Silvano, Marcello Lajolo, Gianluca Palermo. "Low Power Networks-on-Chip" SPRINGER, 1st Edition., 2011, ISBN: 978-1-4419-6910-1

BC.3. Stamelakos Ioannis, Xydis Sotirios, Palermo Gianluca, Silvano Cristina. "Variability-Aware Voltage Island Management for Near-Threshold Computing with Performance Guarantees". In "Near Threshold Computing: Technology, Methods and Applications". 2016. Editors: M. Hubner Michael C. Silvano, p. 35-53, Springer, ISBN: 978-3-319-23388-8, doi: 10.1007/978-3-319-23389-5_3

BC.4. Antonino Tumeo, Marco Ceriani, Gianluca Palermo, Marco Minutoli, Vito G. Castellana, Fabrizio Ferrandi. "Real-time considerations for rugged embedded systems". In "Rugged Embedded Systems: Computing in Harsh Environments". 2016 Editors: Augusto Vega, Pradip Bose, Alper Buyuktosunoglu. p. 39-56, Elsevier Inc., ISBN: 9780128026328, doi: 10.1016/B978-0-12-802459-1.00003-8

BC.5. Cristina Silvano, William Fornaciari, Gianluca Palermo, Vittorio Zaccaria, Fabrizio Castro, Marcos Martinez, Sara Bocchio, Roberto Zafalon, Prabhat Avasare, Geert Vanmeerbeeck, Chantal Ykman-Couvreur, Maryse Wouters, Carlos Kavka, Luka Onesti, Alessandro Turco, Umberto Bondi, Giovanni Mariani, Hector Posadas, Eugenio Villar, Chris Wu, Fan Dongrui, Zhang Hao and Tang Shibin, "MULTICUBE: Multi-Objective Design Space Exploration of Multi-Core Architectures", Lecture Notes in Electrical Engineering, Vol. 57 - Selected Papers from VLSI 2010 Annual Symposium, N. Voros et al. (Eds.), pp. 47 to 63 - 2011.

BC.6. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, A. Di Biagio, E. Speziale, M. Tartara, D. Melpignano, J.-M. Zins, D. Siorpaes, H. H?bert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Leupers, H. Meyr, J. Ansari, P. M?h?nen and B. Vanthournout, "2PARMA: Parallel Paradigms and Run-time Management Techniques for Many-Core Architectures", Lecture Notes in Electrical Engineering, Vol. 57 - Selected Papers from VLSI 2010 Annual Symposium, N. Voros et al. (Eds.), pp. 65 to 79 - 2011.

BC.7. Giovanni Mariani, Chantal Ykman-Couvreur, Prabhat Avasare, Geert Vanmeerbeeck, Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria, "Design Space Exploration for Run-time Management of a Reconfigurable System for Video Streaming", Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.), pp. 189 to 204 - 2011.

BC.8. Carlos Kavka, Luka Onesti, Enrico Rigoni, Alessandro Turco, Sara Bocchio, Fabrizio Castro, Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria, Giovanni Mariani, Fan Dongrui, Zhang Hao, and Tang Shibin, Design Space Exploration of Parallel Architectures, Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.), pp. 171 to 187 - 2011.

BC.9. Prabhat Avasare, Chantal Ykman-Couvreur, Geert Vanmeerbeeck, Giovanni Mariani, Gianluca Palermo, Cristina Silvano and Vittorio Zaccaria, "Design Space Exploration Supporting Run-Time Resource Management", Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.), pp. 93 to 107 - 2011.

BC.10. Gianluca Palermo, Cristina Silvano, Vittorio Zaccaria, Enrico Rigoni,Carlos Kavka, Alessandro Turco and Giovanni Mariani, "Response Surface Modeling for Design Space Exploration of Embedded Systems", Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.), pp. 75 to 91 - 2011.

BC.11. Enrico Rigoni, Carlos Kavka, Alessandro Turco, Gianluca Palermo,Cristina Silvano, Vittorio Zaccaria, Giovanni Mariani, "Optimization Algorithms for Design Space Exploration of Embedded Systems", Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.), pp. 51 to 73 - 2011.

BC.12. Cristina Silvano, William Fornaciari, Gianluca Palermo, Vittorio Zaccaria, Fabrizio Castro, Marcos Martinez, Sara Bocchio, Roberto Zafalon, Prabhat Avasare, Geert Vanmeerbeeck, Chantal Ykman-Couvreur, Maryse Wouters, Carlos Kavka, Luka Onesti, Alessandro Turco, Umberto Bondi, Giovanni Mariani, Hector Posadas, Eugenio Villar, Chris Wu, Fan Dongrui and Zhang Hao, "The MULTICUBE Design Flow", Multi-objective Design Space Exploration of Multiprocessor SoC Architectures, Cristina Silvano, William Fornaciari, Eugenio Villar (Eds.), pp. 3 to 17 - 2011.

BC.13. Leandro Fiorin, Gianluca Palermo, Cristina Silvano. "Security in NoC", in "Networks-on-Chips: Theory and Practice". Fayez Gebali, Haytham Elmiligi, and M.Watheq El-Kharashi (Eds.), Taylor & Francis Group LLC - CRC Press, 2008, pg 157-194.

BC.14. G. Bertoni, Vittorio Zaccaria, L. Breveglieri, Matteo Monchiero, Gianluca Palermo. "A Power Attack Methodology to AES Based on Induced Cache Misses: Procedure, Evaluation and Possible Countermeasures", in "New Trends in Cryptographic Systems". N. Nedjah and L.M. Mourelle (Eds.), Nova Science Publishers, 2006, pg 37-52.

BC.15. D. Barretta, L. Breveglieri, P. Maistri, M. Monchiero, L. Negri, A. Pagni, G. Palermo, M. Sami, C. Silvano, O. Villa, R. Zafalon, "Low Power Architectures", in "Mobile Information Systems - Infrastructure and Design for Adaptivity and Flexibility - The MAIS Approach". B. Pernici (ed.), Springer, 2006, pp 177-206.

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IC.1. Emanuele Vitali, Anton Lokhmotov, Gianluca Palermo: "Dynamic Network selection for the Object Detection task: why it matters and what we (didn't) achieve". International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS), 2021

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