Curriculum Vitae

Personal information

First name/ Surname **Marcello Mariani**

Work experience

2/2023 → now

Distinguished Member of Technical Staff, DRAM Device & Cell Technology , device characterization team leader.

Managing the device characterization team in charge of cell development for next generation DRAM technologies

1/2018 → 2/2023

Distinguished Member of Technical Staff, Emerging memories R&D, device characterization team leader.

In charge of process integration, from proof of concept to pre-industrialization phase, of emerging memories technologies; leading a team in charge of device electrical characterization

1/2015 → 1/2018

Senior Member of Technical Staff, Emerging memories R&D

In charge of process integration, from proof of concept to pre-industrialization phase, of emerging memories technologies, with a particular focus on reliability.

Name and address of employer **Micron Technology**, Via Trento 30, Vimercate, Italy

Type of business or sector Semiconductors

Dates **7/2013 →1/2015**

Occupation or position held ***Senior Member of Technical Staff, Process Integration Team Leader***

Main activities and responsibilities	. Leading a group in charge of process integration for advanced memories. Main responsibilities are: • Technology roadmap definition for advanced memories, with a particular focus on process integration • Advanced memories process integration development, from architecture foundation to pre-industrialization phase • Coordination of process development "task forces", including cooperation with external research institutes and/or universities • Process transfer form R&D to production sites.
Name and address of employer	**Micron Technology**, Via C. Olivetti 2, 20041 Agrate Brianza (Italy)
Type of business or sector	Semiconductors
Dates	**01/09/2008 → now**
Occupation or position held	***Contract Professor***
Main activities and responsibilities	Running the "Microelectronic technologies" course for EE graduate students.
Name and address of employer	Politecnico di Milano, Piazza L. da Vinci, 32 - 20133 Milano (Italy)
Type of business or sector	University
Dates	**01/10/2000 → 30/09/2002**
Occupation or position held	***Process development engineer***
Main activities and responsibilities	Development of plasma etching processes.
Name and address of employer	ST Microelectronics, Via C. Olivetti 2, 20041 Agrate Brianza (Italy)
Type of business or sector	Semiconductors
Dates	**01/02/2000 → 09/10/2000**
Occupation or position held	***Researcher***
Main activities and responsibilities	In charge of designing and testing micro-strip silicon detectors for the CMS (Compact Muon Solenoid) experiment, that is now taking place at the LHC (Large Hadron Collider) accelerator in CERN (European Centre for Nuclear Research), Geneve.
Name and address of employer	INFN (National Insitute for Nuclear Physics) Edificio C - Polo Fibonacci Largo B. Pontecorvo, 3 - 56127 Pisa
Type of business or sector	University
Dates	**01/10/1999 → 31/12/1999**
Occupation or position held	***Researcher***
Main activities and responsibilities	Worked in prof. Fukuda's lab on crystalline fibres growth by micro-pulling-down technique. Growth of YAG and LuAG fibres for laser applications.
Name and address of employer	Institute for Materials Research, Tohoku University, 2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan
Type of business or sector	University

Education and training

Dates	**01/10/1994 → 27/09/1999**
Title of qualification awarded	Master Degree, Physics (full marks, 110/110)

Principal subjects/occupational skills covered	Solid state physics, physics of semiconductor devices. Thesis title “Automatic quantum efficiency measurements on commercial CCD cameras”.
Name and type of organisation providing education and training	Università degli studi di Pisa
Level in national or international classification	ISCED 5

Personal skills and competences

Mother tongue(s) **Italian**

Other language(s)

Self-assessment	Understanding				Speaking				Writing	
European level (*)	Listening		Reading		Spoken interaction		Spoken production			
English	C2	Proficient	C2	Proficient	C2	Proficient	C2	Proficient	C2	Proficient

(*) Common European Framework of Reference for Languages

Patents and publication

Patents

1. Memory array with leakers, patent pending
2. Memory array configuration for shared word lines, patent pending
3. Memory devices having adjacent memory cells with mitigated disturb risk, patent pending
4. Memory device having a diagonally opposite gate pair per memory cell, patent pending
5. Differential storage in memory arrays, patent pending
6. Memory device assembly with redistribution layer between transistors and capacitors, patent pending
7. Formation for memory cells, patent pending
8. Ferroelectric memory arrays with low permittivity dielectric barriers, patent pending
9. Ferroelectric memory architecture with gap region, patent pending
10. Techniques to manufacture ferroelectric memory devices, patent pending
11. Integrated assemblies having shield lines between neighboring transistor active regions, US-11636882-B2
12. Integrated Assemblies and Methods of Forming Integrated Assemblies, US-20230014289-A1
13. Integrated Assemblies and Methods of Forming Integrated Assemblies, US-20230014289-A1
14. Transistors, memory arrays, and methods used in forming an array of memory cells individually comprising a transistor, US-11557591-B2
15. Integrated Assemblies and Methods of Forming Integrated Assemblies, US-20230010846-A1
16. Memory Devices and Methods of Forming Memory Devices, US-20220285392-A1
17. Array Of Vertical Transistors, An Array Of Memory Cells Comprising An Array Of Vertical Transistors, And A Method Used In Forming An Array Of Vertical Transistors, US-20220278001-A1

18. Array of vertical transistors, an array of memory cells comprising an array of vertical transistors, and a method used in forming an array of vertical transistors, US-11373914-B2
19. Array Of Capacitors, An Array Of Memory Cells, Method Used In Forming An Array Of Memory Cells, Methods Used In Forming An Array Of Capacitors, And Methods Used In Forming A Plurality Of Horizontally-Spaced Conductive Lines, US-20220190004-A1
20. Integrated Transistors Having Gate Material Passing Through a Pillar of Semiconductor Material, and Methods of Forming Integrated Transistors, US-20220037533-A1
21. Methods of Incorporating Leaker Devices into Capacitor Configurations to Reduce Cell Disturb, and Capacitor Configurations Incorporating Leaker Devices, US-20220020756-A1
22. Memory Devices and Methods of Forming Memory Devices, US-20210391334-A1
23. Ferroelectric memory cell recovery, US 9697913 B1
24. Methods of forming an array of gated devices, US9224738 B1
25. Controlling the circuitry and memory array relative height in a phase change memory feol process flow, US8154006B2
26. Method of fabricating a charge trap NAND flash memory, US8329545
27. Shallow Trench Isolation For A Memory, US8097506B2
28. Self-aligned vertical bipolar junction transistor for phase change memories, US7985959B2
29. Method for manufacturing non volatile memory cells integrated on a semiconductor substrate, US20070202647A1
30. Method of making a floating gate non-volatile MOS semiconductor memory device with improved capacitive coupling, US8008701B2
31. Process for the formation of dielectric isolation structures, US20080213970A1
32. Method for manufacturing semiconductor integrated circuit structures, EP1387395B1
33. Array of Gated Devices and Methods of Forming An Array of Gated Devices, US10153194B2
34. Memory devices comprising magnetic tracks individually comprising a plurality of magnetic domains having domain walls and methods of forming a memory device comprising magnetic tracks individually comprising a plurality of magnetic domains having..., US10147497B2
35. Method of Fabricating a Charge Trap NAND Flash Memory Device, US9224873B2
36. Methods of Forming Electrical Contacts, US2012302052A1
37. Semiconductor Devices and Fabrication Method, US9245987B2
38. Methods of forming gated devices, US8962465B2
39. Method, system and device for recessed contact in memory array, US9111857B2
40. Forming Three Dimensional Isolation Structures, US20120126374A1
41. Vertical devices and methods of forming, US8530312B2
42. Double patterning method for creating a regular array of pillars with dual shallow trench isolation, US8921196B2

Publications

- **Engineering Domain-Wall Motion in Co–Fe–B/MgO Ultrathin Films with Perpendicular Anisotropy Using Patterned Substrates with Subnanometer Step Modulation**; A. Digiacomo, R. Mantovan, N. Vernier, T. Devolder, K. Garcia, G. Tallarida, M. Fanciulli, A. Lamperti, B. Ocker, L. Baldi, M. Mariani, and D. Ravelosona; Phys. Rev. Applied 10, 064053
- **Front-End Processes, chapter in "Nanoelectronics: Materials, Devices, Applications"**; Marcello Mariani; May 2, 2017 ,Wiley

- **Perpendicular magnetic anisotropy in Ta/CoFeB/MgO systems synthesized on treated SiN/SiO2 substrates for magnetic memories**; R.Mantovan, A. Lamperti, G.Tallarida, L.Baldi, M.Mariani, B.Ocker,S-M.Ahn,I. Barisic, D.Ravelosona; Thin Solid Films, Volume 533, 30 April 2013, Pages 75-78
- **The role of the substrate in the high energy boron implantation damage recovering** ; I.Mica, L.Di Piazza, L.Laurin, M.Mariani, A.G.Mauri, M.L.Polignano, E.Ricci, F.Sammiceli, G.Spoldi, ;Materials Science and Engineering B 159-160:168-172
- **The evolution of the ion implantation damage in device processing;** M. L. Polignano, I. Mica, V. Bontempo, F. Cazzaniga, M. Mariani, A. Mauri, G. Pavia, F. Sammiceli, G. Spoldi; J Mater Sci: Mater Electron (2008) 19(Suppl 1): 182.
- **Poly-CMP integration for sub 90 nm self-aligned floating gate flash memories**; Marcello Mariani, Luca Canevari, Claudia Romanelli; International Conference on Planarization/CMP Technology · October 25 – 27, 2007 Dresden
- **The Role of the Interstitial Oxygen in the Recovery and Evolution of the Boron Implantation Damage;** I. Mica, M.L. Polignano, F. Cazzaniga, L.Di Piazza, M. Mariani, E. ricci, F.Sammiceli,S. Speranza; Solid State Phenomena, Vols. 156-158, pp. 269-274, 2010
- **A 65nm NOR Flash Technology with 0.042µm² Cell size for High Performance Multilevel Application;** G.Servalli, D.Brazzelli, E.Camerlenghi, G.Capetti, S.Costantini, C.Cupeta, D.DeSimone, A.Ghetti, T.Ghilardi, P.Gulli, M.Mariani, A.Pavan, R.Somaschini ; IEEE IEDM Tech. Dig. pp. 2.5.1-2.5.4, 2005
- **Raman spectroscopy of strain in subwavelength microelectronic devices;** Emiliano Bonera, Marco Fanciulli, Marcello Mariani**;** Appl. Phys. Lett. 87, 111913 (2005)
- **Results with microstrip detectors produced by ST Microelectornics for the CMS tracker**; G. Segneri, L. Borrello, R. Dell'Orso, S. Dutta, P.G. Fallica, M. Mariani, A. Messineo, A. Starodumov, L. Teodorescu, G. Tonelli et al..; Nucl.Instrum.Meth. A476 (2002) 729-733
- **Comprehensive study of the effects of irradiation on charge collection efficiency in silicon detectors**; L. Borrello, R. Dell'Orso, S. Dutta, S. Gennai, M. Mariani et al.; Nucl. Instrum. Meth. A461:178-181, 2001

Autorizzo al trattamento dati ai sensi del GDPR 2016/679 del 27 aprile 2016 (Regolamento Europeo relativo alla protezione delle persone fisiche per quanto riguarda il trattamento dei dati personali).

Autorizzo la pubblicazione del Curriculum Vitae sul sito istituzionale del Politecnico di Milano (sez. Amministrazione
Trasparente) in ottemperanza al D. Lgs n. 33 del 14 marzo 2013 (e s.m.i.).