Curriculum vitae prof. William Fornaciari – Politecnico di Milano, Italy (POLIMI)

PERSONAL INFORMATION:

Family name, First name: FORNACIARI, WILLIAM

Type of Profile: Academic Professor

Email: william.fornaciari@polimi.it

Lab at POLIMI: http://heaplab.deib.polimi.it

Linkedin: https://www.linkedin.com/in/william-fornaciari-9818285/

EDUCATION

1992	PhD in Ingegneria Informatica ed Automatica (Computer Engineering) Politecnico di Milano, Milano, Italy
1989	MSc in Ingegneria Elettronica, *Summa cum laude* Politecnico di Milano, Milano, Italy

CURRENT POSITION(S)

2001 –	Associate Professor Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB) Politecnico di Milano, Milano, Italy

PREVIOUS POSITIONS

1995 – 2001	Assistant Professor Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB) Politecnico di Milano, Milano, Italy
1992 – 2005	Post-doc researcher, Head of the Embedded Systems Unit and Scientific Mentor CEFRIEL (www.cefriel.it, it is one of the technology transfer centers of Politecnico di Milano), Milano, Italy

FELLOWSHIPS AND AWARDS

2019	Winner of the Switch2Product (S2P) - Innovation Challenge competition in 2019. Organizers: Technology Transfer Office (TTO) of the Politecnico di Milano, Deloitte - Officine Innovazione and PoliHUB. https://s2p.it
2019	IEEE Transactions on Control Systems Technology "OUTSTANDING PAPER AWARD" - Event-Based Power/Performance-Aware Thermal Management for High-Density Microprocessors, IEEE Transactions on Control Systems Technology, Vol. 26, No. 2, pages 535-550, 2018.
2016	Technology Transfer Award: "Insurance Telematics for Reduced Cost of Ownership". HiPEAC Network of Excellence. www.hipeac.net
2002	Senior Member of the IEEE (Institute of Electrical and Electronics Engineers, USA)
2012	Best Paper Award at the IEEE Symp. on System-on-Chip (SoC)
2011	Member of the EU Network of Excellence HiPEAC. www.hipeac.net
2000	"Giovani Ricercatori (Young Researchers)" Competitive grant for the scientific project: "Riuso di celle IP (Intellectual Properties) per progetti hardware: metriche di analisi e modelli di costo". Politecnico di Milano.
1998	Best Paper Award Conf. IEEE- ICCD'98 (International Conference on Computer Design)
1995	IEEE Circuits and Systems Society – "Certificate of Appreciation" for services rendered as General Chairman, Intl Workshop on Hardware/Software co-design 1995.
1995	Best Paper Award Conf. ICONIP'95 (Inl Conf on Neural Information Processing)
1992	Best Paper Award: Intl IEEE Conference IJCNN'92. (Int. Joint Conf on Neural Networks)

SUPERVISION OF GRADUATE STUDENTS AND POSTDOCTORAL FELLOWS

Currently	3 postdocs / 4 PhD students / 4 MSc students being supervised
2006 – 2018	6 postdocs / 6 finished PhD Theses / around 30 MSc Theses, all from Politecnico di Milano
1995 – 2005	Co-supervisor of 4 PhDs currently working in Academia with tenure tracks.

TEACHING ACTIVITIES

2004 –	Embedded Systems, English, Politecnico di Milano, Italy and University of Parma, Italy
2006 –	Advanced Operating Systems, English, Politecnico di Milano, Italy
2016 -	Reti Logiche (Digital Systems Design), Italian, Politecnico di Milano, Italy
2000 – 2004	Various Master courses in: operating systems, computer architectures, digital systems design, fundamentals of computer science at Politecnico di Milano and University of Parma. Italy

2003 - 2004 "Networked Operating Systems", MSc in EE & CS, Univ. of Chicago at Illinois (US)

2006-2008 Lecturer "Executive MBA on "Information and Communication Technologies", organized by School of Management of Politecnico di Milano

2006-2007 Lecturer post graduate master course on "International Business Engineering (FHINK)" organized by Finmeccanica Spa

ORGANISATION OF SELECTED SCIENTIFIC MEETINGS

2020 Member of the **Scientific Committee** of the conferences: Design Automation Conference (DAC); Design Automation and Test in Europe (DATE); CASES (ES_WEEK) International Conference on Compilers, Architectures, and Synthesis for Embedded Systems; ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED); Euromicro Conference on Digital System Design (DSD); NORCAS; Workshops at HiPEAC (PARMA-DITAM), **Program Chair**: IEEE IGSC 2020 - international green and sustainable computing, IEEE International Conference on Omni-layer Intelligent systems. COINS 2020 - IEEE International Conference on Omni-layer Intelligent systems.

2019 Member of the **Scientific Committee** of the conferences: Design Automation Conference (DAC); Design Automation and Test in Europe (DATE); CASES (ES_WEEK) International Conference on Compilers, Architectures, and Synthesis for Embedded Systems; ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED); Euromicro Conference on Digital System Design (DSD); ARCS; NORCAS; Workshops at HiPEAC (PARMA-DITAM, AISTECS2019), **Program Chair** of International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), INTESA workshop at ESWEEK. **Chair of the track** "Critical System Design" at COINS Conference.

2018 **Program Chair** of the INTESA workshop at ESWEEK and of PARMA-DITAM @ HiPEAC. Member of the **Scientific Committee** of the conferences: Design Automation and Test in Europe (DATE), Euromicro Conference on Digital System Design (DSD), NORCAS, Workshops at HiPEAC (PARMA-DITAM)

2014 **Track Chair** of the Intl Conf. on Design, Automation and Test in Europe (DATE). Mar 24-28 2014, Dresden, Germany.

2011 **General chair** of the 24th Int.l. Conference on Architecture of Computing Systems (ARCS 2011). Feb 22-25, 2011, Como, Italy.

2010 **Program Chair** of the 1st Int.l. Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (PARMA). Feb 22-25, 2010, Hannover, Germany.

2010-2018 Member of the Scientific committees and sometimes organizer of special session/tracks of these main conferences Design Automation Conference (DAC), Design Automation and Test in Europe (DATE), Euromicro Conference on Digital System Design (DSD), ARCS (Int.l. Conference on Architecture of Computing Systems,) PARMA-DITAM workshop at HiPEAC, IEEE Int.l. Conference on Field Programmable Logic and Applications, IEEE Int.l. Symposium on System-on-Chip.

INSTITUTIONAL RESPONSIBILITIES

2019 Member of the CINI special interest group on high performance computing

2018 - POLIMI representative in the board of the National Lab on Embedded Systems & Smart Manufacturing **(**www.consorzio-cini.it)

REVIEWING ACTIVITES

- He participated in the project reviewing board appointed by the EU Commission for the EU Artemis project (JU Grant agreement number 10023) iFEST.
- He participated in the project reviewing board appointed by the Cyprus Ministry of Education and Culture.
- He was appointed by the The Netherlands Organization for Scientific Research (NWO) to evaluate project proposals submitted to the competitive grant scheme Vici - Innovational Research Incentive Scheme (twice, also in 2019)

2020 Member of the Editorial Board of the Elsevier Int. Journal "Sustainable Computing: Informatics and Systems (SUSCOM)"

1995 - Reviewer of ACM/IEEE/Euromicro conferences and Journal, such as: TRVLSI, MICPRO, TCAD, TACO, TRCOMP, DAC, DATE, DSD, ARCS, NORCAS, PARMA-DITAM

2018-2019 Co-Editor of the book, William Fornaciari and Dimitrios Soudris, "Harnessing Performance Variability in Embedded and High-performance Many/Multi-core Platforms - A Cross-layer

Approach", Springer International Publishing, AG, NY, 2018 (on-line), 2019 (printed)

2018 Guest Editor of the Special Issue on Mobile Systems Technologies of Microprocessors and Microsystems Journal, Elsevier, 2018.

2016 Co-editor of the book, Cristina Silvano, William Fornaciari and Dimitrios Soudris: "Run-time Management techniques for Many-core Architectures", Springer International Publishing, AG, NY, 2016.

2014 Co-editor of the book, Cristina Silvano, William Fornaciari and Eugenio Villar "Multi-Objective Design Space Exploration of Multiprocessor Soc Architectures: The Multicube Approach", Springer International Publishing, November 2014.

COUNCIL OF SCIENTIFIC SOCIETIES

2002 Senior member of IEEE computer society

1993-1998 Director of the board of the VHDL Italian User group

2011 Member of the EU Network of Excellence HiPEAC. www.hipeac.net

Ongoing and main past grants

prof. William Fornaciari – Politecnico di Milano, Italy (POLIMI)

H2020 On-going Grants:

Project Title	*Funding source*	*Period*	*Role*
RECIPE, EU project n. 612801137. Reliable power and time constrains aware predictive management of heterogeneous exascale systems	H2020-FETHPC-2017	2018-2021	Project Coordin.
APROPOS, Int. Training Networks, GA n. 956090, Approximate Computing for Power and Energy Optimisation	H2020-MSCA-ITN-2020	2020-2024	PI

H2020 Past Grants:

Project Title	*Funding source*	*Period*	*Role*
SAFECOP, EU project ID 692529. Safe cooperating cyber physical systems	H2020-EU.2.1.1.7.-ECSEL	2016-2019	PI
M2DC, EU project ID 688201. Modular Microserver DataCentre	H2020-EU.2.1.1.	2016 - 2019	PI
MANGO, European project ID 671668. exploring Manycore Architectures for Next-GeneratiOn HPC systems	H2020-EU.1.2.2.-FET Proactive	2015 – 2019	PI

FP7 Past Grants:

Project Title	*Funding source*	*Period*	*Role*
EU project HARPA, n. 612069. Harnessing Performance Variability	FP7-ICT-2013-10	2013-2016	Project Coordin.
EU project CONTREX, n. 611146	FP7-ICT-2013-10	2013-2016	PI
EU project 2PARMA, n.248716 PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures	FP7-ICT-2009-4	2010-2013	Technical Manager
EU project MULTICUBE, n.216693	FP7-ICT-2007-1	2010-2013	WP Leader
EU project COMPLEX, n. 247999.	FP7-ICT-2009-4	2009-2013	PI

Principal Investigator in charge of the activities of the local unit at the technology transfer center (CEFRIEL)-Politecnico di Milano

- Framework Contract For Impact Analysis Contract No.30-CE-0029513/00-42 Funded by EU Commission Information Society and Media Directorate General Specific Contract No. 30-CE – 0206456/00-95 (Call for Tender No. 964-2005). Project Title: WING. (Jan 2007-Dec 2009, 36m)
- EU FP6-IST-2005-2.5.3 Embedded Systems project WASP, ID: FP6-IST-034963.(Sep 2006 - Aug 2010, 48m).

- EU FP5-IST Project POET, ID FP5-IST-2000-30125. (Sep 2001-2004, 36m)
- EU Esprit Project SEED. n. 22133.(Jul 1996-Sep 1997, 15m)

Member of the key personnel of the local unit at Politecnico di Milano

- European Institute of Innovation and Technology (EIT), Digital Program 2015, activity n. A15257. (Jan 2015-Dec 2015, 12m).
- ARTEMIS (Call 2009) Project SMECY, n. 100230. (Feb 2010-Jan 2013, 36m).
- South-Eastern European Information Telecommunication Cohesion Initiative (SEITCO) project CADSES, ID. 3B042.(Nov 2003-Oct 2005, 24m). Local Technical Leader.

NATIONAL (ITALIAN) PROJECTS

Member of the key personnel of the Politecnico di Milano

- Italian MIUR-FIRB project MAIS (Jan 2003-Jul 2006, 36m).
- Italian MIUR-FIRB project ART-DECO, (Jan 2006 - Dec 2009, 36m). Italian MIUR-PRIN project WiSe DeMon, prot. 2007J4SKYP_005. (Jul 2008-Jul 2010, 24m).
- **Main investigator and responsible** of the project named "progetto dal titolo Riuso di celle IP (Intellectual Properties) per progetti hardware: metriche di analisi e modelli di costo", which has been winner of the Polimi Research Contest "Giovani Ricercatori", year 2000.
- Italian CNR 97/99 Coordinated Research project "Metodologie e Strumenti per la progettazione Automatica di Circuiti e Sistemi Digitali a Basso Consumo di Potenza".
- Italian CNR 97/98 Coordinated Research project MADESSII.

Industrial Projects - Principal investigator and Financial responsible of the contracts

- Customer: STMicroelectronics. Title: Optimizing mobile Linux in terms of power and performance. (Jun 2009- Dec 2009, 6m)
- Customer: STMicroelectronics. Title: Analisi di architetture hardware e software per lo sviluppo di sistemi MPSoC per sistemi multimediali e telecom. (May 2006- May 2007, 12m)
- Customer: CEFRIEL. Title: Messa a punto di metodologie per la progettazione di sistemi dedicati (Mar 2006-Mar 2007, 12m)
- Customer: CEFRIEL. Title: Messa a punto di metodologie per la progettazione di sistemi dedicati (Feb 2005-Feb 2006, 12m)
- Customer: CEFRIEL Title: Messa a punto di metodologie per la progettazione di sistemi embedded (Dec 2003-Dec 2004, 12m)

Track-record
prof. William Fornaciari (POLIMI)
Twelve recent representative publications. Out of 300 publications (Source MIUR, www.miur.it).

Note that the practice in my research sector is to follow an alphabetic ordering of the authors or, when the scientist is the senior leader of a research group, his/her name is placed as the last author.

1. Zoni, Davide, Cremona, Luca, **Fornaciari,** William (2020). All-digital control-theoretic scheme to optimize energy budget and allocation in multi-cores. IEEE TRANSACTIONS ON COMPUTERS, vol. 1, p. 1, ISSN: 0018-9340, doi: 10.1109/TC.2019.2963859
2. D.Zoni, L.Cremona, W.**Fornaciari**, All-digital energy-constrained controller for general-purpose accelerators and CPUs. IEEE Embedded Systems Letters, 2019. doi: 10.1109/LES.2019.2914136
3. A.Barenghi, W.**Fornaciari**, G.Pelosi, D.Zoni, "Scramble Suit: A Profile Differentiation Countermeasure to Prevent Template Attacks", IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, 2019. doi: 10.1109/TCAD.2019.2926389
4. F.Reghenzani, G.Massari, W. **Fornaciari,** "The Real-Time Linux Kernel: A Survey on PREEMPT_RT", ACM COMPUTING SURVEY, 2019. Vol 52, art. 18, pp 1-36, DOI: 10.1145/3297714.
5. D. Zoni, A. Barenghi, G. Pelosi, W. **Fornaciari** (2018). A Comprehensive Side-Channel Information

Leakage Analysis of an In-Order RISC CPU Microarchitecture. ACM TRANSACTIONS ON DESIGN AUTOMATION OF ELECTRONIC SYSTEMS, vol. 23, p. 1-30, ISSN: 1084-4309, doi: 10.1145/3212719.

6. Davide Zoni, Luca Colombo, William **Fornaciari** (2018). DarkCache: Energy-performance Optimization of Tiled Multi-cores by Adaptively Power Gating LLC Banks. ACM TRANSACTIONS ON ARCHITECTURE AND CODE OPTIMIZATION, vol. 15, p. 1-25, ISSN: 1544-3566, doi: 10.1145/3186895
7. Leva, Alberto, Terraneo, Federico, Giacomello, Irene, **Fornaciari**, William (2018). Event-Based Power/Performance-Aware Thermal Management for High-Density Microprocessors. IEEE TRANSACTIONS ON CONTROL SYSTEMS TECHNOLOGY, vol. 26, p. 535-550, ISSN: 1063-6536, doi: 10.1109/TCST.2017.2675841
8. Zoni, Davide, Canidio, Andrea, **Fornaciari**, William, Englezakis, Panayiotis, Nicopoulos, Chrysostomos, Sazeides, Yiannakis (2017). BlackOut: Enabling fine-grained power gating of buffers in Network-on-Chip routers. JOURNAL OF PARALLEL AND DISTRIBUTED COMPUTING, vol. 104, p. 130-145, ISSN: 0743-7315, doi: 10.1016/j.jpdc.2017.01.016
9. Zoni, Davide, Flich, José, **Fornaciari**, William (2015). CUTBUF: Buffer Management and Router Design for Traffic Mixing in VNET-based NoCs. IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS, vol. 99, p. 1-14, ISSN: 1045-9219, doi: 10.1109/TPDS.2015.2468716
10. Bellasi, Patrick, Massari, Giuseppe, **Fornaciari**, William (2015). Effective runtime resource management using linux control groups with the BarbequeRTRM framework. ACM TRANSACTIONS ON EMBEDDED COMPUTING SYSTEMS, vol. 14, p. 1-17, ISSN: 1539-9087, doi: 10.1145/2658990
11. Brandolese Carlo, **Fornaciari** William, Pomante Luigi, Salice Fabio, Sciuto Donatella (2006). Affinity-driven system design exploration for heterogeneous multiprocessor SoC. IEEE TRANSACTIONS ON COMPUTERS, vol. 55, p. 508-519, ISSN: 0018-9340, doi: 10.1109/TC.2006.66
12. Brandolese, Carlo, Salice, Fabio, **Fornaciari**, William, Sciuto, Donatella (2002). Static power modeling of 32-bit microprocessors. IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, vol. 21, p. 1306-1316, ISSN: 0278-0070, doi: 10.1109/TCAD.2002.804104

2. Granted and submitted patents

- A computing platform and method for synchronize the prototype execution and simulation of hardware devices, Date: 5/6/2020 n° patent 102020000013390 (ITA)
- Una piattaforma informatica per prevenire attacchi ai canali laterali, Date: 11/5/2020, n° patent 102020000010531 (IT)
- (PCT/IT2016/000037, WO2017/141277) Dispositivo elettronico per il controllo di temperatura e prestazioni di calcolo di almeno una unità di elaborazione e relativo sistema e metodo di controllo. 2016, 2017. In 2018 it has been filed the application for patenting in USA and EU (EP 16722713.1, 17.09.2018). Submitted patents to US and EU.
- US 8,452,992 B2 [May 28, 2013] S. Bosisio, P. Bellasi, M. Carnevali, D. Siorpaes, William Fornaciari (inventors) Title: Power Management using constraints in multi-dimensional parameter space. Applicant: STMicroelectronics, IT.
- An encoder/decoder architecture for buses capable of minimizing power consumption by reducing the switching activity. EP1 150 467 A1, 2011 with ST Microelectronics.

3. Invited presentations to internationally established conferences and/or international advanced schools

In the past 10 years, Keynote Speaker / Invited talks in the following main events:

- HiPEAC 2020 Tutorial “A Run-time Managed Programming Approach to Computing Continuum”
- Keynote speech. “Opportunities and challenges to design an open-hardware SoC in the IoT era”, PDP 2019, 27th Euromicro on Parallel, Distributed and Network Based processing, Pavia, February 14th, 2019.
- Invited Speaker “Creating a startup: a step-by-step “design experience” from the perspective of an academic co-founder”, TISU - Workshop on Transfer to Industry and Start-Ups, Hipeac 2017. Stockolm, Sweden, January 25, 2017.
- Keynote speech. "Targeting Applications and Platform Variability Challenges: The BarbequeRTRM approach", 8th Int.l. Workshop on Reconfigurable Communication Centric Systems-on-Chip - ReCoSoC 2013, Darmstadt, Germany, July 11th, 2013.
- Keynote speech. "An Accurate Simulation Framework for Thermal Explorations and Optimizations", DAC 2015 Workshop "System-to-Silicon Performance Modeling and Analysis - Power, Temperature and Reliability", June 7, 2015 - San Francisco, CA, USA.

- Invited Talk. “From Embedded systems to high performance computing”. Chiesi Farmaceutici Spa Annual Meeting, June 9, 2016, Parma Italy.
- Invited Talk. "HARPA: Harnessing Performance Variability", Hipeac Computing System Workshop (CSW) & Block Review, Thematic Session on FP7 projects HARPA, CLERECO and EXCESS; Convergence, Perspectives and Joint Vision. Oslo, May 4-8, 2015.
- Invited Talk. “Management of mixed criticality and reliability at run-time: the HARPA approach in Thematic Session on mixed criticality/reliability - Real-Time and Reliability Cross Domain Challenges”. HiPEAC CSW and block review, Barcelona May 13-15 2014.
- Invited Talk. "Run-time management of multi-core architectures using the BBQ framework: Targeting Applications and Platform “Variability” Challenges", ChipEx14, Conf. of the Israeli Microelectronics Industry, Tel Aviv, Apr 30, 2014.
- Invited Talk. "Overview of competencies on Embedded System and Computer Architecture", Fostering Innovation for Cyber-Physical Systems, Advanced Computing & Manufacturing: Opportunities under Horizon 2020 LEIT-ICT Work Programme 2014/15, Feb 19-20, Brussels, 2014.
- Invited Talk. Day 1 - Success stories of technology adoption - 2PARMA, Day 2- Session 2: Embedded Multi-Core Platforms - taking stock of achievements and economic perspectives: 2PARMA and HARPA , Cyber-Physical Systems: Uplifting Europe's innovation capacity, Brussels, Oct 29-30, 2013.
- Invited Talk. "2PARMA Project", REFLECT and 2PARMA Fall 2012 School: Programming Paradigms for MultiCore Embedded Systems, Freustadt, Germany, Oct 2-5, 2012.
- Invited Talk. "System-Wide run-time resource management for multi-many cores in the 2PARMA Project" - HiPEAC Computing Systems Week; Session on Power-Efficiency and Program Correctness Analysis for Scalable Multicores, April 2012, Göteborg, Sweden, Apr 24-25, 2012.
- Invited Talk. “2PARMA Overview”, HiPEAC Innovation Event - Session on FP7 European Projects, May 3-5, 2010 Edinburgh, UK.
- Invited Talk. “System-wide run-time resources management”, NEC-Labs at Princeton, NJ, USA, Dec 16th, 2009.
- Invited Talk. “System-wide run-time resources management” Princeton University, NJ, USA, Dec 15th, 2009.
- Invited Talk. "Digital Vehicular Dashboard", Telemobility Forum Europeo 2007. Monza, Italia, 14-15 Novembre, 2007.
- Invited Talk. "Software: modello di sviluppo nelle applicazioni per gli apparecchi elettrodomestici", Istituto italiano del marchio di qualità (IMQ), May 18 2007, Milan, Italy.

5. Examples of leadership in industrial innovation or design.

- Head of the embedded systems unit at the CEFRIEL (www.cefriel.it) Technology Transfer center of Politecnico di Milano, Italy, co-developing commercial and innovative products (1992-2005)
- I won the 2016 Technology Transfer Award: "Insurance Telematics for Reduced Cost of Ownership". HiPEAC Network of Excellence (www.hipeac.net) for the output of the CONTREX EU-Project.
- In 2013 I co-founded the SME “IBT Solutions” and in 2016 another spin-off “IBT Systems srl” (www.ibtsystems.it) whose focus is the design of products and embedded applications for automotive, industrial and environmental monitoring. More than 500.000 vehicles are using our technology.
- In 2019- after winning the the Switch2Product (S2P) - Innovation Challenge competition, his team is participating to the acceleration program of PoliHUB to create a startup
- In 2020 co-ownership of a pre-SEED funding by the Venture Capital “Poli 360” for the development of a Proof of concept for further product industrialization.

Si autorizza il trattamento dei dati personali ai sensi e per gli effetti del ai sensi del D.lgs. 196 del 30 giugno 2003 e s.m.i. e del Regolamento Europeo in materia di protezione dei dati personali, n. 679/201

Milano, July 1st, 2020

prof. William Fornaciari