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PUBBLICATIONS STATS:

Journals

24 Journals: **12** ACM/IEEE Transactions

Conferences

120 papers: **1**DAC, **4** ICCAD, **1** FPGA, **1** ITC, **11** DATE, **6** ASPDAC, **4** CODES/ISSS.

Book Chapters

12 book chapter contributions.

BIBLIOMETRICS INDEXES

Google scholar:

2267 number of citations,

26 h-index,

Most cited paper: 201 Nane Razvan, Sima Vlad-Mihai, Pilato Christian, Choi Jongsok, Fort Blair, Canis Andrew, Chen Yu Ting, Hsiao Hsuan, Brown Stephen, Ferrandi Fabrizio, Anderson Jason, Bertels Koen. A Survey and Evaluation of FPGA High-Level Synthesis Tools. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 35, p. 1591-1604, 2016.

Scopus:

18 h-index, **133** documents, **1240** citations.

EDUCATION

- Ph.D. in Information and Automation engineering at Politecnico di Milano, Italy. Sept 1997. Title: "Metodologie di supporto alla progettazione di sistemi digitali testabili", Advisor: Prof. Donatella Sciuto. The thesis was partially supported by a governmental sholarship received from Ministero dell'Istruzione, dell'Università e della Ricerca (MIUR).
- Laurea cum laude in Electronic Engineering at Politecnico di Milano, Italy. Oct 1992. Thesis title: "Analisi della collaudabilità per architetture VLSI: metodologie per una valutazione automatica", Advisor Prof. Mariagiovanna Sami. The thesis was partially supported by a grant received from ITALTEL SIT.

PROFESSIONAL EXPERIENCE

- 2002-present Associate Professor at the Dipartimento di Elettronica e Informazione, Faculty of Engineering, Politecnico di Milano.
- 1999-2002 Assistant professor at the Dipartimento di Elettronica e Informazione, Faculty of Engineering, Politecnico di Milano.
- 1998-99 " Research Assistant" at Dipartimento di Elettronica e Informazione, Politecnico di Milano.
- 1994-2001 Contract professor of Fundamental of Computer Science, Faculty of Engineering, at the University Cattaneo (LIUC), Varese.
- 1996-99 Contract professor of Fundamental of Computer Science, Faculty of Economy, at the University Cattaneo (LIUC), Varese.
- 1992-93, 1997-98 Consultant for the Dipartimento di Elettronica e Informazione, Politecnico di Milano.

RESEARCH INTERESTS

- Methodologies for the high-level synthesis of C based specification on FPGA-based platforms
- Methodologies for high-performance computing on FPGA based platforms
- Methodologies for synthesis of dynamically reconfigurable systems on FPGA-based platforms
- Methodologies for synthesis and optimization of complex VLSI designs
- Methodologies for testing and verifying complex VLSI devices
- System-level modeling, specification and verification through simulation of hardware/software systems
- Methodologies for design space exploration and partitioning of system-level specifications based on static and dynamic metrics in order to identify the best hardware/software mapping and software tasks allocation on multiprocessor platforms
- Methodologies and tools for synthesis and simulation of multi-processor-based platforms

AWARDS

- Best Paper Award EURO-VHDL '96 for the paper titled "BDD-based Testability Estimation of VHDL Designs" presented at IEEE/ACM European Design Automation Conference and Euro-VHDL, Ginevra, Switzerland, September 16-20 1996.
- PhD thesis awarded with "1997 Prize for Engineering and Technology – THE DIMITRIS N.CHORAFAS FOUNDATION", 26-08-1997.
- Best Paper Award DATE '99 for the paper titled "Symbolic functional vector generation for VHDL specifications" presented at IEEE/ACM DATE '99 – Design, Automation and Test in Europe, Munich, Germany, March 9-12 1999.

PROFESSIONAL ACTIVITIES

- Steering Committee member of International Conference on Field Programmable Logic and Applications (FPL) since 2011.

- General Chair of International Conference on Field Programmable Logic and Applications (FPL), 2010.
- General Chair of Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms –2011.
- Topic Chair or Co-Chair in different subcommittees of Design Automation and Test in Europe (DATE) from 2006 to 2018.
- Topic Co-Chair of "Synthesis and design space exploration" subcommittee of International Conference on Hardware/Software Codesign and System Synthesis (ISSS-CODES) 2011.
- TPC member of ISIS-1997, IC-SAMOS-2006-08, NAS2010, DATE2006-18, GLSVLSI-2011,ISSS-CODES-2006-2019, ReConFig-2012-17 ,ARCS-2012-2018, VIPES-2013-15, DAC-2013-15, ASP-DAC-2017-19, CF-2016-2018, FPL-2010-19,ICCD19

TUTORIALS

- "BAMBU: An open-source framework for research in high-level synthesis" at 27th International Conference on Field-Programmable Logic and Applications, Ghent, Belgium (September 2017).
- "BAMBU: An open-source framework for research in high-level synthesis" at International Conference on Field-Programmable Technology, Melbourne Australia (December 2017).
- PNNL-2019 Workshop – "Bambu: FPGA Programming for Complex Parallel Applications", Richland, WA USA, February 2019.

TEACHING

2003-2018 LOGIC DESIGN - Computer Engineering - Undergraduate level.

2014-present DIGITAL SYSTEMS DESIGN METHODOLOGIES - Computer Engineering - Master level. Taught in English.

2013-present ADVANCED ALGORITHMS AND PARALLEL PROGRAMMING - Computer Engineering - Master level. Taught in English.

Member of "Collegio docenti dottorato - INGEGNERIA DELL'INFORMAZIONE" of Politecnico di Milano from 01-01-2004 al 31-12-2009.

I taught a PhD course titled "Algoritmi e strutture dati per la progettazione e la verifica di sistemi complessi/ Algoritmi per la Progettazione VLSI" - INGEGNERIA DELL'INFORMAZIONE from 2004 to 2009.

OPEN SOURCE PROJECTS

I started the PandA project in 2004. Within this framework I'm actively working on methodologies supporting high-level synthesis of hardware accelerators, on parallelism extraction for embedded systems, on hardware/software partitioning and mapping, on metrics for performance estimation of embedded software applications and on dynamic reconfigurable devices.

From time to time, I contributed to the FloPoCo project. FloPoCo is a generator of arithmetic cores (Floating-Point Cores, but not only) for FPGAs (but not only). FloPoCo has been even successfully integrated into the high-level synthesis tool bambu distributed with PandA framework.

EUROPEAN COMMISSION PROJECTS

I worked in these European funded projects as researcher:

- REQUEST – Reuse and quality estimation: advanced VHDL based design methodology for quick system development
- ICODES – Interface and Communication based Design of Embedded Systems
- hArtes – Holistic Approach to Reconfigurable Real Time Embedded Systems
- Synaptic – SYNthesis using Advanced Process Technology Integrated in regular Cells, IPs, architectures, and design platforms
- Faster – Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration
- SAVE – Self-Adaptive Virtualization-Aware High-Performance/Low-Energy Heterogeneous System Architectures
- HERMES-SP – H2020 Hermes Scientific Pathfinder

In addition, in Synaptic I worked as scientific coordinator for Politecnico di Milano.

EUROPEAN SPACE AGENCY PROJECTS

In the following ESA projects, I've worked as scientific coordinator/advisor:

- ESA/ESTEC/Contract No. 22167/09/NL/JK. Cache Optimization for LEON Analysis (COLA) (2010).
- ESA/ESTEC/Contract N. 4000100797 – Development of methodologies and tools for predictable, real-time LEON-DSP based embedded systems (2011).
- ESA/ESTEC/Contract Call-Off Order 4 "Multicore and Schedulability Analysis" for TASTE project (2014).
- ESA/ESTEC/ 4000121154/17/NL/LF – Compact Reconfigurable AvionicsModel Based Avionic Design (2019).

NATIONAL PROJECTS

I coordinated in the context of "Progetto Giovani Ricercatori" the research titled "Definizione di una metodologia di collaudo per dispositivi elettronici descritti a livello algoritmico" and funded by Politecnico di Milano, 2000.

I was scientific coordinator for Politecnico di Milano of project "Nu-Specs (nu-tech speech engine with CUDA support)" – Bando 2008 giovane tecnologo-Intervento 1.1.1.04.03 – Marche innovazione

I'm involved in an ASI funded project named Hermes Technological Pathfinder which involves two Polimi departments DEIB and DAER.

OTHER PROJECTS

I'm Co-Principal Investigator on project "Design Automation for Data Analytics" accepted in the Intel Hardware Accelerator Research Program v2. Started 24-11-2016 and jointly developed with Pacific Northwest National Laboratory.

I'm Co-Principal Investigator on project "Hardware parallelization of cores accessing memory with irregular access patterns" accepted in the Intel Hardware Accelerator Research Program v2. Started 24-11-2016.

JOURNAL PUBLICATIONS

[A1] M.Bombana, G.Buonanno, P.Cavalloro, F.FERRANDI, D.Sciuto, G.Zaza,
"ALADIN: A Multi-Level Testability Analyzer for VLSI System Design",
IEEE Transaction on Very Large Scale Integration (VLSI) Systems,
vol. 2, no. 2, June 1994, pp. 157-171.

[A2] F.FERRANDI,
"Reduction of Fault Detection Costs through a BDD Formalism",
Microprocessing and Microprogramming (The EUROMICRO Journal),
vol. 8 n. 40 Ed. Elsevier Science, 1994, pp. 841-844.

[A3] C.Bolchini, G.Buonanno, F.FERRANDI, D.Sciuto, M.Bombana, P.Cavalloro,
"A Wafer Level Testability Approach Based on an Improved Scan Insertion Technique",
IEEE - Transaction on Components, Packaging, and Manufacturing Technology Part B; Advanced Packaging,
vol. 18, no. 3, August 1995, pp. 438-447.

[A4] F.FERRANDI, F.Fummi, E.Macii, M.Poncino, D.Sciuto,
"Testing Core-Based Digital Systems: A Symbolic Methodology",
IEEE - Design&Test of Computers,
vol. 14, no. 4, October-December 1997, pp. 69-77.

[A5] F.FERRANDI, F.Fummi, E.Macii, M.Poncino, D.Sciuto,
"Symbolic optimization of interacting controllers based on redundancy identification and removal",
IEEE - Transactions on Computer-Aided Design of Integrated Circuits and Systems,
vol. 19, no. 7, July 2000, pp. 760-772.

[A6] A. Antola, F. FERRANDI, V. Piuri, M. Sami,
"Semi-Concurrent Error Detection in Data Paths",
IEEE - Transactions on Computers,
vol. 50, no. 5, May 2001, pp. 449-465.

[A7] R. Cordone, F.FERRANDI, D. Sciuto, R. Wolfler Calvo,
"An Efficient Heuristic Approach to Solve the Unate Covering Problem"
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,
vol. 20, n. 12, December 2001, pp. 1377 – 1388.

[A8] F.FERRANDI, F.Fummi, D.Sciuto,
"Test Generation and Testability Alternatives Exploration of Critical Algorithms for Embedded Applications"
IEEE Transactions on Computers, Volume: 51 Issue: 2 , Feb. 2002 Page(s): 200 –215.

[A9] G. Biasoli, F.FERRANDI, A. Fin, F.Fummi, D.Sciuto
"Behavioral Test Generation for the Selection of BIST Logic"
Journal of Systems Architecture, Elsevier Science Publisher, Vol.47, no.10, 2002.

[A10] Ferrandi, F.; Fummi, F.; Pravadelli, G.; Sciuto, D.;
"Identification of design errors through functional testing"
IEEE Transactions on Reliability,Volume: 52 , Issue: 4 , Dec. 2003 Pages:400 – 412.

[A11] Bruschi F.; Ferrandi, F.; Sciuto, D.;
"A Framework for the Functional Verification of SystemC Models"
International Journal of Parallel Programming. Publisher: Springer Science+Business Media B.V , vol. 33, Dec. 2005, pp. 667-695.

[A12] Christian Pilato, Antonino Tumeo, Gianluca Palermo, Fabrizio Ferrandi, Pier Luca Lanzi, and Donatella Sciuto.
"Improving evolutionary exploration to area-time optimization of FPGA designs".
Journal of Systems Architecture, Volume 54, Issue 11, November 2008, Pages 1046-1057.

[A13] K. Bertels, V.M. Sima, Y. Yankova, G. Kuzmanov, W. Luk, J.G.F. Coutinho, F. Ferrandi, C. Pilato, M. Lattuada, D. Sciuto, A. Michelotti. hArtes: Hardware-Software Codesign for Heterogeneous Multicore Platforms. *IEEE Micro*, vol. 30, p. 88-97, 2010.

[A14] Ferrandi F., Lanzi P.L., Pilato C., Sciuto D., Tumeo A. Ant Colony Heuristic for Mapping and Scheduling Tasks and Communications on Heterogeneous Embedded Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 29, p. 911-924, 2010.

[A15] S. Cecchi, A. Primavera, F. Piazza, F. Bettarelli, E. Ciavattini, R. Toppi, J.G.F. Coutinho, W. Luk, C. Pilato, F. Ferrandi, V.M. Sima, K. Bertels. The hArtes CarLab: A New Approach to Advanced Algorithms Development for Automotive Audio. *AES*, vol. 59, p. 858-869, 2011.

[A16] Lattuada Marco, Pilato Christian, Ferrandi Fabrizio. Performance Estimation of Task Graphs Based on Path Profiling. *International Journal of Parallel Programming*, vol. 44, p. 1-37, 2015.

[A17] Marco Lattuada, Fabrizio Ferrandi. Modeling Resolution of Resources Contention in Synchronous Data Flow Graphs. *Journal of Signal Processing Systems for Signal, Image, and Video Technology*, vol. 80, p. 39-47, 2015.

[A18] Nane Razvan, Sima Vlad-Mihai, Pilato Christian, Choi Jongsok, Fort Blair, Canis Andrew, Chen Yu Ting, Hsiao Hsuan, Brown Stephen, Ferrandi Fabrizio, Anderson Jason, Bertels Koen. A Survey and Evaluation of FPGA High-Level Synthesis Tools. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, p. 1591-1604, 2016.

[A19] Fezzardi, Pietro, Lattuada, Marco, Ferrandi, Fabrizio. Using Efficient Path Profiling to Optimize Memory Consumption of On-Chip Debugging for High-Level Synthesis. *ACM Transactions on Embedded Computing Systems,* vol. 1, p. 1-19, 2017.

[A20] Lattuada Marco, Ferrandi Fabrizio. Exploiting Vectorization in High Level Synthesis of Nested Irregular Loops. *Journal of Systems Architecture*, vol. 75, p. 1-14, 2017.

[A22] Lattuada, Marco, Ferrandi, Fabrizio, Perrotin, Maxime. Data Transfers Analysis in Computer Assisted Design Flow of FPGA Accelerators for Aerospace Systems. *IEEE Transactions on Multi-Scale Computing Systems*, vol. 4, p. 3-16, 2018.

[A23] Pietro Fezzardi, Christian Pilato, Fabrizio Ferrandi. Enabling Automated Bug Detection for IP-based Designs using High-Level Synthesis. *IEEE Design & Test*, 35(5), pp. 54-62, 2018.

[A24] Marco Lattuada and Fabrizio Ferrandi. 2019. A Design Flow Engine for the Support of Customized Dynamic High Level Synthesis Flows. ACM Transactions on Reconfigurable Technology and Systems. 1, 1 (Accepted July 2019), 24 pages.

CONFERENCES PUBLICATIONS

[B1] M.Bombana, G.Buonanno, P.Cavalloro, F.Ferrandi, D.Sciuto, G.Zaza,
"An Expert Solution to Functional Testability Analysis of VLSI Circuits",
Proc. SEKE 93 – 5th International Conference on Software Engineering and Knowledge Engineering,
San Francisco, California, USA, June 16-18 1993, pp. 263-265.

[B2] M.Bombana, G.Buonanno, P.Cavalloro, F.Ferrandi, D.Sciuto, G.Zaza,
"Reduction of Fault Detection Cost through Testable Design of Sequential Architectures with Signal Feedbacks",
Proc. IEEE DFT 93 – IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems,
Venice, Italy, October 27-29 1993, pp. 223-230.

[B3] M.Bombana, G.Buonanno, P.Cavalloro, F.Ferrandi, D.Sciuto, G.Zaza,
"Cycles Analysis for Testability of WSI Sequential Architectures",
Proc. IEEE WSI 94 – 6th IEEE International Conference on Wafer Scale Integration,
San Francisco, California, USA, January 19-21 1994, pp.188-197.

[B4] D.Sciuto, C.Bolchini, G.Buonanno, F.Ferrandi, M.Bombana, P.Cavalloro, G.Zaza
"Towards WSI Testable Devices: an Improved Scan Insertion Technique"
Proc. IEEE WSI 95 – 7th IEEE International Conference on Wafer Scale Integration,
San Francisco, California, USA, January 18-20 1995, pp. 339-348.

[B5] C.Bolchini, G.Buonanno, F.Ferrandi, D.Sciuto, M.Bombana, P.Cavalloro,
"Assessment of functional testability properties from VHDL descriptions"
Proc. VHDL-FORUM EUROPE Spring '95 - Working Conference,
Nantes, France, April 24-25 1995, pp. 84-95.

[B6] G.Buonanno, F.Ferrandi, D.Sciuto,
"Data-Path Efficient Testability Analysis Based on BDDs",
Proc. IEEE ISCAS '95 – IEEE International Symposium on Circuits and Systems,
Seattle, Washington, USA, April 29 - May 3 1995, pp. 2012-2015.

[B7] F.Ferrandi, F.Fummi, E.Macii, M.Poncino, D.Sciuto,
"Test Generation for Networks of Interacting FSMs Using Symbolic Techniques",
Proc. IEEE GLS-VLSI '96 – The 6th Great Lake Symposium on VLSI,
Ames, Iowa, USA, March 22-23 1996, pp. 208-213.

[B8] F.Ferrandi, F.Fummi, E.Macii, M.Poncino, D.Sciuto,
"Symbolic Optimization of FSM Networks Based on Sequential ATPG Techniques",
Proc. ACM/IEEE DAC – 33rd ACM/IEEE Design Automation Conference,
Las Vegas, Nevada, USA, June 3-7 1996, pp. 467-470.

[B9] F.Ferrandi, F.Fummi, E.Macii, M.Poncino, D.Sciuto,
"BDD-Based Testability Estimation of VHDL Designs",
Proc. IEEE EURO-DAC '96 – European Design Automation Conference and EURO-VHDL,
Geneva, Switzerland, Sept. 16-20 1996, pp. 444-449.
Best Paper Award EURO-VHDL '96.

[B10] F.Ferrandi, F.Fummi, E.Macii, M.Poncino, D.Sciuto,
"Simplifying Sequential Gate-Level Test Generation Through Exploitation of High-Level Information",
Proc. ETW '96 – IEEE European Test Workshop,
Sete Montpellier, France, June 12-14, 1996, pp. 154-158.

[B11] F.Ferrandi, F.Fummi, R.Bevacqua, L.Guerrazzi,
"Implicit Test Sequences Compaction for Decreasing Test Application Cost",
Proc. IEEE ICCD '96 – IEEE International Conference on Computer Design: VLSI in Computers, and Processors,
Austin, Texas, USA, Oct. 7-9 1996, pp. 384-389.

[B12] F.Ferrandi, F.Fummi, R.Bevacqua, L.Guerrazzi,
"Sequential Test Compaction for Test Embedding",
Proc. OLTW '96 – 2nd IEEE International On-Line Testing Workshop,
San-Jean De-Luz Biarritz, France, July 8-10 1996, pp. 229-230.

[B13] G.Buonanno, F.Ferrandi, D.Sciuto,
"Testability Analysis of Pipelined Data Path",
Proc. IEEE ISIS '96 – IEEE International Conference on Innovative System in Silicon,
Austin, Texas, U.S.A, October 9-11, 1996, pp. 259-268.

[B14] M.Bombana, P.Cavalloro, F.Ferrandi,
"Good Practice for Property Verification in the design of Telecom Applications",
Proc. ACM/IEEE ASP-DAC '97 – ACM/IEEE Asia and South Pacific Design Automation Conference,
Chiba, Japan, January 28-31 1997, pp. 167-172.

[B15] G.Buonanno, F.Ferrandi, L.Ferrandi, F.Fummi, D.Sciuto,
"How an "Evolving" Fault Model Improves the Behavioral Test Generation",
Proc. IEEE GLS-VLSI '97 – The 7th Great Lake Symposium on VLSI,
Ames, Iowa, USA, March 22-23 1997, pp.124-129.

[B16] A.Allara, M.Bombana, P.Cavalloro, F.Ferrandi,
"Requirements and experiences for formal design of telecom systems",
Proc. Workshop on Formal Design of Safety Critical Embedded Systems,
Munich, Germany, April 16-18 1997.

[B17] G.Buonanno, F.Ferrandi, F.Fummi, D.Sciuto, P.Cavalloro,
"An Extended Testing Methodology for VHDL Based High-Level Design",
Proc. VHDL Forum for CAD in Europe,
Toledo, Spain, April 20-25 1997, pp. 63-74.

[B18] M.Bacis, G.Buonanno, F.Ferrandi, F.Fummi, L.Gerli, D.Sciuto,
"Application of a Testing Framework to VHDL Descriptions at Different Abstraction Levels",
Proc. IEEE ICCD '97 – IEEE International Conference on Computer Design: VLSI in Computers and Processors,
Austin, Texas, 13-15 October, 1997, pp. 654-659.

[B19] F.Ferrandi, F.Fummi, E.Macii, M.Poncino, D.Sciuto,
"Power Estimation of Behavioral VHDL Descriptions",
Proc. IEEE DATE '98 – Design, Automation and Test in Europe,
Paris, France, February 24-26, 1998, pp. 762-766.

[B20] F.Ferrandi, F.Fummi, L.Pozzi, M.Sami,
"Configuration-Specific Test Pattern Extraction for Field Programmable Gate Arrays",
Proc. IEEE DFT 97 – IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,
Paris, France, October 20-22, 1997, pp. 85-93.

[B21] F.S.Bietti, F.Ferrandi, F.Fummi, D.Sciuto,
"VHDL Testability Analysis based on Faults Clustering and Implicit Faults Injection",
Proc. IEEE GLS-VLSI '98 – The 8th Great Lakes Symposium on VLSI,
Lafayette, Louisiana, 19-21 February, 1998, pp. 237-242.

[B22] F.Ferrandi, A.Macii, E.Macii, M.Poncino, R.Scarsi, F.Somenzi,
"Layout-oriented Synthesis of PTL Circuits based on BDDs",
Proc. IWLS'98 – 1998 IEEE/ACM International Workshop on Logic Synthesis,
Lake Tahoe, California, 7-10 June , 1998.

[B23] M.Bombana, P.Cavalloro, F.Ferrandi, F.Fummi, D.Sciuto,
"Implicit Testability Techniques for VHDL Based ASIC Design",
Proc. ETW'98 – IEEE European Test Workshop,
Barcelona, Spain, May 27-29, 1998, pp. 133-134.

[B24] F.Ferrandi, F.Fummi, D.Sciuto,
"Behavioral Test Generation for Test Embedding",
Proc. IOLTW '98 – 4th IEEE Int. On-Line Testing Workshop,
Capri, Italy, July 6-8, 1998, pp. 100-104.

[B25] D.Corvino, I.Epicoco, F.Ferrandi, F.Fummi, D.Sciuto,
"Controller and Data-Path Separation by VHDL Restructuring",
Proc. Forum on Design Languages – FDL'98: VHDL Users' Forum in Europe (VUFE),
Lausanne, Switzerland, Sept. 7-11 1998, pp. 237-243.
Selezionato fra i migliori articoli della conferenza e invitato per la pubblicazione su libro edito da Kluwer Academic Publishers.

[B26] M.Bombana, P.Cavalloro, F.Ferrandi, F.Fummi, D.Sciuto,
"The REQUEST Testability methodology for VHDL based ASIC design",
Proc. Forum on Design Languages – FDL'98: VHDL Users' Forum in Europe (VUFE),
Lausanne, Switzerland, Sept. 7-11 1998, pp. 209-215.

[B27] D.Corvino, I.Epicoco, F.Ferrandi, F.Fummi, D.Sciuto,
"Automatic VHDL Restructuring for RTL Synthesis Optimization and Testability Improvement",
Proc. IEEE ICCD '98 – IEEE International Conference on Computer Design: VLSI in Computers and Processors,
Austin, Texas, USA, Oct. 5-7 1998, pp. 436-441.

[B28] F.Ferrandi, F.Fummi, D.Sciuto,
"Implicit Test Generation for Behavioral VHDL Models",
Proc. IEEE ITC'98 – IEEE International Test Conference,
Washington, D.C., USA, Oct. 18-23, 1998, pp. 587-596.

[B29] F.Ferrandi, A.Macii, E.Macii, M.Poncino, R.Scarsi, F.Somenzi,
"Symbolic algorithms for layout-oriented synthesis of pass transistor logic circuits Symbolic Algorithms for Layout-Oriented PTL Synthesis",
Proc. ACM/IEEE ICCAD'98 – ACM/IEEE International Conference on Computer-Aided Design,
San Jose, CA, November 8 - 12, 1998, pp. 235 -241.

[B30] F.Ferrandi, F.Fummi, L.Gerli, D.Sciuto,
"Symbolic functional vector generation for VHDL specifications"
Proc. IEEE DATE '99 – Design, Automation and Test in Europe,
Munich, Germany, March 9-12,1999, pp. 442-446.
Best Paper Award DATE '99.

[B31] M.Brera, F.Ferrandi, D.Sciuto, F. Fummi,
"Increase the Behavioral Fault Model Accuracy Using High-Level Synthesis Information",
Proc. IEEE DFT 99 – IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,
Albuquerque, New Mexico, November 1-3, 1999, pp. 174-180.

[B32] R. Cordone, F.Ferrandi, D. Sciuto, R. Wolfler Calvo,
"An Efficient Heuristic Approach to Solve the Unate Covering Problem"
Proc. IEEE DATE 2000 – Design, Automation and Test in Europe,
Paris, Franch, March 27 - 30, 2000, pp. 364-371.

[B33] F. Ferrandi, G. Ferrara, G. Fornara, F. Fummi, D. Sciuto,
"Testability Alternatives Exploration through Functional Testing",
Proc. IEEE VTS 2000 – 18th IEEE VLSI Test Symposium,
Montreal, Canada, April 30- May 4, 2000, pp. 124-129.

[B34] F. Ferrandi, A.Fin, F.Fummi, D.Sciuto,
"An Application of Genetic Algorithms and BDDs to Functional Testing",
Proc. IEEE ICCD'00 – IEEE International Conference on Computer Design: VLSI in Computers and Processors,
Austin, Texas, September 17-20, 2000, pp.48-56.

[B35] G. Biasoli, F. Ferrandi, A.Fin, F.Fummi, D.Sciuto,
"BIST Architectures Selection Based on Behavioral Testing",
Proc. IEEE DFT'00 – IEEE International Symposium on Defect and Fault Tollerance in VLSI Systems,
Yamanashi, Japan, October 25-27, 2000, pp. 292-298.

[B36] M. Beardo, F. Bruschi, F. Ferrandi, D. Sciuto,
"An Approach to Functional Testing of VLIW Architectures",
Proc. IEEE HLDVT'00 – 5th IEEE International Workshop on High Level Design Validation and Test,
Berkeley, California, USA, November 8-10, 2000, pp. 29-33.

[B37] F. Ferrandi, G. Ferrara, D. Sciuto, A. Fin, F. Fummi,
"Functional Test Generation for Behaviorally Sequential Models",
Proc. IEEE DATE 2001 – Design, Automation and Test in Europe,
Munich, Germany, March 13-16, 2001, pp. 403-410.

[B38] A. Allara, M. Bombana, P. Cavalloro F. Ferrandi,
"Requirements for synthesis-oriented modeling in SystemC",
Proc. FDL'01 – Forum on Design Languages,
Lyon, France, September 3-7, 2001.

[B39] F. Ferrandi, M. Rendine, D. Sciuto,
"Functional verification for SystemC descriptions using constraint solving",
Proc. IEEE DATE 2002 – Design, Automation and Test in Europe,
Paris, France, March 4-8, 2002.

[B40] F. Bruschi, M. Chiamenti, F. Ferrandi, D. Sciuto,
"Error simulation based on the SystemC design description language",
Proc. IEEE DATE 2002 – Design, Automation and Test in Europe,
Paris, France, March 4-8, 2002.

[B41] M. Bombana, F. Bruschi, F. Ferrandi, D. Sciuto,
"SystemC Specification of a Telecom PCI-compatible Interface",
Proc. IEEE DATE 2002 – Design, Automation and Test in Europe,
Paris, France, March 4-8, 2002.

[B42] Francesco Bruschi, F. Ferrandi
"Synthesis of complex control structures from behavioral SystemC models"
Proc. IEEE DATE 2003 – Design, Automation and Test in Europe,
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