Christian Pilato

No Tenure-Track Assistant Professor
Dipartimento di Elettronica, Informazione e Bioingegneria
Politecnico di Milano – Via Ponzio 34/5, 20133 Milano, Italy
Born on December 28th, 1982 in Busto Arsizio (VA), Italy
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Highlights

- More than 12 years of academic research on Electronic Design Automation (EDA), parallel programming, embedded architectures, hardware design, and hardware security
  - More than 6 years (in total) spent abroad, including: PhD visit in Denmark (2009, 6 months), HiPEAC Collaboration Grant in Sweden (2012, 3 months), Postdoc contracts in USA (2013, ∼3 years) and Switzerland (2016, 2 years), Visiting Researcher in The Netherlands (2016, 5 months) and USA (2017, 9 months).
  - Visiting researcher in both industry (Nangate A/S, Denmark) and academia (Chalmers Institute of Technology, Sweden; Delft University of Technology, The Netherlands; New York University, USA)
- Published widely in international journals and conferences
  - 15 journal papers (1 ACM Transaction, 5 IEEE Transactions, 2 IEEE magazines)
  - 41 conference papers (3 ACM/IEEE DAC papers, 1 single-author paper)
  - 2 papers with more than 100 citations each; 25 papers with more than 10 citations (i10-index = 25)
- Actively involved in the organization of conferences, workshops, and tutorials in the area of heterogeneous system-on-chip architectures
  - Special Session and Tutorial Chair of IEEE International Conference on Computer Design (2015-ongoing)
  - Co-Organizer of a PhD Summer School on Cyber-Physical Systems (2017-ongoing)
  - Program Committee Member of major conferences in FPGA and EDA (DAC, DATE, CASES, FPL)
  - Keynote speaker at the IEEE/IFIP International Conference on Field Programmable Technology (2017)
  - Guest editor for a special issue in ACM Transactions on Embedded Computing Systems (2015)
  - Program Chair of the IEEE/IFIP Conference on Embedded and Ubiquitous Computing (2014)
- Actively involved in several DARPA, SRC and EU-funded projects, for both technical and managerial aspects
  - Currently PI of one grant on hardware security (total PI funding: ∼€49K)
  - Collaborated on writing grant proposals (∼€790K awarded to the research group) and period reports
  - Attended most of technical meetings with project partners and annual reviews with the European Commission and the C-FAR Center
- Habilitation to the function of *Associate Professor* in *Information Processing Systems* (Sector: 09/H1) (June 2018)

Education

- **Ph.D. in Information Technology** at Politecnico di Milano *Feb. 2011*
  Thesis Title: *Design Methodologies for Improving Embedded Systems with Hardware Accelerators*
  Advisor: *Fabrizio Ferrandi – Donatella Sciuto*
- **M.Sc. in Computer Science Engineering** at Politecnico di Milano *Apr. 2007*
  Thesis title: *High Level Synthesis with Area Constraints for FPGA Designs: An Evolutionary Approach*
  Advisor: *Fabrizio Ferrandi* – Grade: 110/110

Research Experience

- **Junior Assistant Professor** *Jun. 2018* – current
  Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy
  – High-level synthesis for hardware security; design of heterogeneous System-on-Chip architectures.
- **Research Fellow** *Sept. 2017 – May 2018*
  Center of Cybersecurity, New York University, USA (*Ramesh Karri and Siddharth Garg*)
  – High-level synthesis for hardware security.

- **Postdoctoral Researcher** *Feb. 2017 – May 2018*
  Faculty of Informatics, Università della Svizzera italiana, Switzerland (*Francesco Regazzoni*)
  – Design methodologies for security-aware high-level synthesis, security metrics for cyber-physical systems.
- **Visiting Research Scientist** *Sept. 2016 – Jan. 2017*
  Department of Microelectronics, Delft University of Technology, The Netherlands (*Edoardo Charbon*)
  – Design of FPGA controllers for SPAD chips.
- **Visiting Research Scientist** *Jun. 2016 – Aug. 2016*
  Faculty of Informatics, Università della Svizzera italiana, Switzerland (*Francesco Regazzoni*)
  – Design methodologies for security-aware heterogeneous architectures.
- **Postdoc Research Scientist** *Sept. 2013 – May 2016*
  Department of Computer Science, Columbia University, USA (*Luca P. Carloni*)
  – Design and integration of hardware accelerators for heterogeneous architectures (including FPGA prototypes, CPU-FPGA platforms, and SoCs), with emphasis on memory-related aspects.
- **Postdoc Research Assistant** *Jun. 2011 – Sept. 2013*
  Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy (*Donatella Sciuto*)
  – Hardware-software methodologies for the design of partially reconfigurable architectures; high-level synthesis methods for memory-intensive applications; profiling techniques to support automatic parallelization.
- **Visiting Researcher** *Sept. 2012 – Dec. 2012*
  Department of Computer Science, Chalmers University of Technology, Sweden (*Georgi Gaydadjiev*)
  – Integration of polymorphic register files for high-performance dataflow computing.
- **Visiting Researcher** *Dec. 2009 – May 2010*
  Nangate A/S, Denmark (*Martin Elhøj*)
  – Design of application-specific standard-cell libraries to improve circuit manufacturing.
- **Research Assistant** *Jun. 2007 – Dec. 2007*
  Dipartimento di Elettronica ed Informazione, Politecnico di Milano, Italy (*Donatella Sciuto*)
  – Development of hardware-software co-design methods for heterogeneous architectures.

Qualifications

- **Italian National Scientific Qualification** *June 26, 2018 – June 26, 2024*
  Habilitation to the function of *Associate Professor* in *Information Processing Systems* (Sector: 09/H1).
- **Italian National Engineering License** *2008*
  Professional practice examination in *Computer Engineering*.

Awards and Honors

- Xilinx Zynq UltraScale+ MPSoC ZCU106 Evaluation Kit (FPGA development board) donated by Xilinx Inc. for research on "hardware security and high-level synthesis".
- Collaboration grant (5K€) by HiPEAC European Network of Excellence for the research "Adaptive and heterogeneous computing systems" with Chalmers University of Technology, Gothenburg, Sweden (2012)
- Ph.D. fully funded by a scholarship from STMicroelectronics (2008–2010)

List of Selected Publications

Refereed Journal Publications

1. K. Basu, S.M. Saeed, C. Pilato, M. Ashraf, M.T. Nabeel, K. Chakrabarty, R. Karri, "CAD-Base: An Attack Vector into the Electronics Supply Chain," in *ACM Transactions on Design Automation of Electronics Systems (TODAES)*, vol. 24, no. 4, pp. 1-30, July 2019.
   [doi: http://dx.doi.org/10.1145/3315574]
2. C. Pilato, K. Wu, S. Garg, R. Karri, F. Regazzoni. "TaintHLS: High-Level Synthesis For Dynamic Information Flow Tracking," in *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 38, no. 5, pp. 798-808, May 2019.
   [doi: http://dx.doi.org/10.1109/TCAD.2018.2834421]
3. C. Pilato, K. Basu, F. Regazzoni, R. Karri. "Black-Hat High-Level Synthesis: Myth or Reality?," in *IEEE Transactions on Very Large Scale Integration Systems*, vol. 27, no. 4, pp. 913-926, April 2019.
   [doi: http://dx.doi.org/10.1109/TVLSI.2018.2884742]

4. P. Fezzardi, C. Pilato, F. Ferrandi. "Enabling Automated Bug Detection for IP-based Designs using High-Level Synthesis," in *IEEE Design & Test Magazine*, vol. 35, no. 5, pp. 54-62, October 2018.
[doi: http://dx.doi.org/10.1109/MDAT.2018.2824121]
5. C. Ciobanu, C. Pilato, G. Gaydadjiev, D. Sciuto. "The Case for Polymorphic Registers in Dataflow Computing," in *International Journal of Parallel Programming*, vol. 46, no. 6, pp. 1185–1219, December 2018.
[doi: http://dx.doi.org/10.1007/s10766-017-0494-1]
6. C. Pilato, P. Mantovani, G. Di Guglielmo, L.P. Carloni, "System-Level Optimization of Accelerator Local Memory for Heterogeneous Systems-on-Chip," in *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 36, no. 3, pp. 435-448, March 2017.
[doi: http://dx.doi.org/10.1109/TCAD.2016.2611506]
7. R. Nane, V.-M. Sima, C. Pilato, J. Choi, B. Fort, A. Canis, Y.T. Chen, H. Hsiao, S. Brown, F, Ferrandi, J. Anderson, K. Bertels. "A Survey and Evaluation of FPGA High-Level Synthesis Tools," in *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 35, no. 10, pp. 1591-1604, October 2016.
[doi: http://dx.doi.org/10.1109/TCAD.2015.2513673]
8. M. Lattuada, C. Pilato, F. Ferrandi. "Performance Estimation of Task Graphs based on Path Profiling," in *International Journal of Parallel Programming*, vol. 44, no. 4, pp. 735-771, August 2016.
[doi: http://dx.doi.org/10.1007/s10766-015-0372-7]
9. F. Ferrandi, P.L. Lanzi, C. Pilato, D. Sciuto, A. Tumeo, "Ant Colony Heuristic for Mapping and Scheduling Task and Communications on Heterogeneous Embedded Systems," in *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 29, no. 6, (2010), pp. 911-924.
[doi: http://dx.doi.org/10.1109/TCAD.2010.2048354]

Refereed Conference Publications

10. C. Pilato, F. Regazzoni, R. Karri, S. Garg. "TAO: Techniques for Algorithmic Obscuration during High-Level Synthesis," in *Proceedings of ACM/IEEE Design Automation Conference* (DAC 2018), San Francisco, CA, USA, June 24-28, 2018, pp. 1-6.
[doi: http://doi.acm.org/10.1145/3195970.3196126]
11. P. Mantovani, E. Cota, K. Tien, C. Pilato, G. Di Guglielmo, K. Shepard, L.P. Carloni, "An FPGA-Based Infrastructure for Fine-Grained DVFS Analysis in High-Performance Embedded Systems," in *Proceedings of ACM/IEEE Design Automation Conference* (DAC 2016), Austin, TX, USA, June 5-9, 2016, pp. 1-6.
[doi: http://doi.acm.org/10.1145/2897937.2897984]
12. G. Di Guglielmo, C. Pilato, L.P. Carloni, "A Design Methodology for Compositional High-Level Synthesis of Communication-Centric SoCs," in *Proc. of ACM/IEEE Design Automation Conf.* (DAC 2014), San Francisco, CA, USA, June 1-5, 2014, pp. 1-6.
[doi: http://doi.acm.org/10.1145/2593069.2593071]

Research Projects

Scientific Committees

Dr. Pilato contributed to the following scientific committees:

- Panel Member for the NSF Graduate Research Fellowship Program (GRFP), 2016

Positions of Trust

Dr. Pilato is currently leading the following grant:

- *Circuit Obfuscation Development and Evaluation*, DARPA CIRCUIT REALIZATION AT FASTER TIMESCALES (CRAFT) PROGRAM (PI funding amount: $55K, ∼€49K) *(approved – defining the contract details)*
  Dr. Pilato is the **Principal Investigator** for Politecnico di Milano in a subcontract agreement with New York University (NYU) and the Boeing Company for the documentation and testing of obfuscation techniques.

Dr. Pilato took a prominent role in the following research project:

- *FASTER (Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration)*, EU FP7 SPECIFIC TARGETED RESEARCH PROJECT (STREP), CONTRACT NO. 287804
  Local project leader: Donatella Sciuto, Politecnico di Milano.
  Dr. Pilato was the **Task Leader** of "Application Task Profiling and Identification of Reconfigurable Cores", which included the work of FORTH (Greece), Chalmers University of Technology (Sweden), Imperial College (UK), Politecnico di Milano (Italy), and Ghent University (Belgium). This task defined design methodologies for reconfigurable systems, involving the concurrent definition of the architecture (i.e., feasible reconfigurable regions) and the application (i.e., corresponding hardware-software partitioning). He collaborated with the local leader and the project coordinator since the definition of the proposal, providing support for all managerial aspects.

Project Participation

In the past, he contributed to the following research projects:

- DARPA CIRCUIT REALIZATION AT FASTER TIMESCALES (CRAFT) PROGRAM
  Local project leaders: Siddharth Garg and Ramesh Karri, New York University (NYU), Steve Fisher (Boeing)
  Dr. Pilato was an NYU external consultant for the definition of high-level design methodologies to obfuscate digital circuits and prevent reverse engineering of the chips to be fabricated. The results of this research produced a tool-flow that has been used for designing an obfuscated chip that has been fabricated at 16nm.
- *CERBERO (Cross-layer modEl-based fRamework for multi-oBjective dEsign of Reconfigurable systems in unceRtain hybRid envirOnments)*, EU H2020 PROJECT, CONTRACT NO. 732105
  Local project leader: Francesco Regazzoni, Università della Svizzera italiana (USI Lugano).
  Dr. Pilato worked on performance indicators and design methodologies to incorporate security concepts into the design of reliable and adaptive cyber-physical systems. This work was mainly done in collaboration with University of Sassari, University of Cagliari, Thales Alenia Space, Centro Ricerche Fiat, Polytechnic University of Madrid, Netherlands Organisation for Applied Scientific Research (TNO), and IBM Haifa.
- *C-FAR (Center for Future Architectures Research)*, STARNET RESEARCH CENTER
  Local project leader: Luca Carloni, Columbia University.
  Dr. Pilato worked on design methodologies and CAD tools for the optimization of the accelerator local memory in heterogeneous SoCs. This also included hardware support for the allocation of massive data sets. This work promoted collaborations with the *Architecture and Design* lab at Columbia University (Martha Kim).
- *ESP (Embedded Scalable Platform)*, DARPA POWER EFFICIENCY REVOLUTION FOR EMBEDDED COMPUTING TECHNOLOGIES (PERFECT) PROJECT, CONTRACT NO. HR0011-13-C-0003
  Local project leader: Luca Carloni, Columbia University.
  Dr. Pilato provided support for the FPGA prototype of the proposed SoC architecture. His work includes the support for the integration of hardware accelerators, the exploration of multiple design implementations, and the characterization of the power consumption for the different components at each voltage-frequency pair. This work has been mainly done in collaboration with the *Bioelectronics Systems* lab at Columbia University (Ken Shepard).
- *Synaptic (SYNthesis using Advanced Process Technology Integrated in regular Cells, IPs, architectures, and design platforms)*, EU FP7 SPECIFIC TARGETED RESEARCH PROJECT (STREP), CONTRACT NO. 248538
  Local project leader: Fabrizio Ferrandi, Politecnico di Milano.
  Dr. Pilato defined a heuristic methodology to automatically identify a minimal set of application-specific standard cells to extend an existing library and improve the manufacturing of digital circuits in state-of-the-art industrial flows. He also provided support through all project's phases since the definition of the proposal.
- *hArtes (Holistic Approach to Reconfigurable real Time Embedded Systems)*, EU FP6 INTEGRATED PROJECT (IP), CONTRACT NO. 035143
  Local project leader: Donatella Sciuto, Politecnico di Milano.
  Dr. Pilato was involved in the definition of compiler-based methodologies (based on GCC) for the semi-automatic parallelization of sequential C-based applications. He also proposed methodologies for defining an early hardware-software partitioning in heterogeneous architectures having limited hardware resources and multiple hardware implementations generated with the support of high-level synthesis.

Research Interests

Dr. Pilato's research focuses on innovative architectures and companion design methodologies, which can be mostly combined with existing commercial tools, for **heterogeneous System-on-Chip (SoC) architectures**. His research covers several design aspects, including (but not limited to):

- design and optimization of accelerator-based computing systems;
- implications concerning hardware security;
- semi-automatic parallelization and hardware/software partitioning;
- design of self-adaptive and reconfigurable architectures;
- physical design and design for manufacturing.

The resulting combined solutions allow the acceleration of various applications (e.g., computer vision, seismic migration,

machine learning, etc.) with significant energy savings. Specifically, his contributions cover the following topics.

High-level synthesis of high-performance accelerators. Dr. Pilato is one of the main developers of BAMBU, an open-source framework for research in *high-level synthesis* (HLS) [IC.19][IC.30] (first release in March 2012, available at http://github.com/ferrandi/PandA-bambu). BAMBU outperforms state-of-the-art academic HLS tools for memory-intensive applications [JR.8]. BAMBU also automatically generates multiple hardware implementations starting from the same C-based specification using a multi-objective design space exploration [JR.1]. Dr. Pilato developed EDA design flows that efficiently combine and coordinate existing tools for the optimization of hardware accelerators [IC.34][JR.9]. He worked on optimizing the communication primitives to avoid deadlock during the computation [IC.34]. He did extensive research on memory aspects since embedded memories are generally responsible for 70-90% of the chip area and 40-50% of the power consumption. First, he proposed an innovative memory architecture for the accelerators that can support, for the first time, almost all the software constructs usually used by software programmers [IC.17][JR.5]. Then, during his 3-month visit at Chalmers University, he worked on the generation of dedicated memory subsystems for the Maxeler platforms [IC.29]. This memory structure allowed the execution of parallel accesses with an application speedup of 40x with respect to solutions using serial memory accesses. Finally, he proposed a methodology, which is complementary to existing HLS tools, to automatically determine an efficient organization of the accelerator memory microarchitecture and minimize the memory footprint while guaranteeing the required memory bandwidth to the computational resources [IC.39][JR.9]. This methodology has been embodied in MNEMOSYNE, an open-source CAD prototype (first released in January 2017, available at https://github.com/chrpilat/mnemosyne) for the generation of multi-bank memories. This combined tool flow allowed the creation of complex accelerators with performance improvements from one to three orders of magnitude with respect to the corresponding software-based solutions. Such accelerators were also included in a prototype chip recently fabricated in a 32nm CMOS technology. After that, he also considered the interaction with the operating system with efficient methods for the allocation of massive sets of data in embedded systems [IC.37]. The expertise in FPGA prototyping has been reused for modeling the effects on autonomous dynamic voltage and frequency scaling in complex heterogeneous SoCs [IC.36]. This solution allowed significant energy savings (up to 75%) and performance improvements (up to 10%) when multiple accelerators are executing concurrently and competing for shared resources.

Hardware security. Dr. Pilato is developing design methods that aim at improving the hardware security of accelerators. In collaboration with NYU, Dr. Pilato defined the challenges for integrating security countermeasures into HLS-generated components to mitigate their area/performance overhead [JR.10]. Dr. Pilato is working on the development and integration of several solutions into BAMBU, showing a novel approach to hardware security based on high-level synthesis. Current solutions include fine-grained hardware support for dynamic information flow tracking [JR.14] and obfuscation techniques to thwart the reverse engineering of the chips to fabricate [IC.40]. In this context, Dr. Pilato has been an external consultant for a DARPA project involving NYU and Boeing for improving the design time of integrated circuits, while increasing their security level. Part of this work has been used to extend BAMBU to implement algorithm-level obfuscation [IC.40]. Dr. Pilato also analyzed the security threats that can be introduced by EDA CAD tools [JR.15] with a focus on high-level synthesis issues (like *planned hardware obsolescence*) [JR.13].

Hardware/software co-design of application-specific systems. The design of heterogeneous SoCs requires determining how to implement computational tasks and communications, depending on a set of constraints of the application and the architecture. Dr. Pilato developed an integrated methodology based on *ant colony optimization* [JR.2] to determine how to efficiently implement each part of the input application, either computational tasks or communications. This method effectively combines the requirements of the application and the constraints of the target architecture, spanning from the automatic generation of specialized accelerators to the system-level design. Given a partitioned application, multiple hardware implementations are combined at the system level. The proposed ACO-based solution uses a constructive approach to generate solutions, exploring the design space more efficiently and reducing the number of unfeasible solutions. In this way, it improves the application performance while respecting the constraints of the target architecture (e.g., limited hardware resources). This research has been included in hArtes, an EU-funded project (2006-2010), where Dr. Pilato worked on the compiler-based analysis of sequential applications for their semi-automatic parallelization and implementation on heterogeneous architectures [JR.3][JR.7].

Self-adaptive and reconfigurable systems. Dr. Pilato extended his ACO-based co-design methodology [JR.2] to take

into account the effects of *partial dynamic reconfiguration* [IC.31] and accordingly specialize the target architecture in terms of static components and reconfigurable regions. This allows the design of adaptive and reconfigurable architectures that are up to three times faster than solutions where the designer was required to manually pre-determine the organization of the architecture. This idea was at the basis of FASTER, an EU-funded project (2011-2014), which is an extension of hArtes to develop methodologies on the top of existing tools for FPGA synthesis in order to include the aspects related to partial dynamic reconfiguration in the early stages of the hardware/software co-design [WS.10][IC.28]. In this project, he coordinated the technical work among five different partners (i.e., FORTH from Greece, Chalmers University of Technology from Sweden, Imperial College from UK, Politecnico di Milano from Italy, and Ghent University from Belgium) to perform high-level analyses and determine the hardware/software partitioning of a parallel application, along with the level of reconfiguration for each hardware component. He also extensively collaborated with Maxeler, which offers a tool flow to optimize algorithms for scientific computation [IC.27]. The work received a Technology Transfer Award in 2012, which is an award given by HiPEAC (an European Network of Excellence) to recognize promising technology transfers between academia and industry.

Logic and physical optimizations with cell-library extensions. Current EDA tools often rely on standard-cell libraries typically optimized with full-custom layouts. However, the quality of these libraries can considerably impact the resulting digital circuits when not properly designed. For this reason, in collaboration with ST Microelectronics (i.e., a leading manufacturer of semiconductors) and NanGate (i.e., an EDA company for standard-cell library optimization, where he was an intern for six months), Dr. Pilato developed a complete design flow for the generation of application-specific standard-cell libraries that can be used in industrial EDA flows for logic and physical synthesis. Specifically, he proposed a methodology to determine which Boolean functions could be implemented with macro gates in order to optimize the circuit. In this way, it is possible to obtain an average reduction of 10% in terms of silicon area and power consumption [IC.12]. This method has been then extended to determine the proper composition of a custom standard-cell library, which allowed a reduction in terms of used cells by almost 90% with negligible impact on the circuits [IC.14]. This research has been at the basis of SYNAPTIC, an FP7-STREP EU project (2009-2013) for improving the manufacturing of digital circuits with regular layouts. With this experience, he recently collaborated in the tape-out and verification of two prototype chips. This allowed the acquisition of an end-to-end expertise in the design of digital circuits.

Complete List of Scientific Publications

Publication Summary

JR	Refereed international journals	15
ED	Editorial contributions	2
IC	Refereed international conferences	41
BI	Refereed chapters in international books	4
WS	Workshops	18

Metrics

Source	Citations	H-Index
Google Scholar	954	15
Scopus	590	11

Highlights

- Most cited paper: [JR.8] (published 2016 – currently 208 citations in Google Scholar and 137 citations in Scopus)
- 20 first-author papers: 5 journal papers (3 IEEE Transactions) and 15 conference papers
- 3 A+ conference papers (1 as first author)
- 141 different paper co-authors

Refereed Journal Publications

JR.15. K. Basu, S.M. Saeed, C. Pilato, M. Ashraf, M.T. Nabeel, K. Chakrabarty, R. Karri, "CAD-Base: An Attack Vector into the Electronics Supply Chain," in *ACM Transactions on Design Automation of Electronics Systems (TODAES)*, vol. 24, no. 4, pp. 1-30, July 2019.
[doi: http://dx.doi.org/10.1145/3315574]

JR.14. C. Pilato, K. Wu, S. Garg, R. Karri, F. Regazzoni. "TaintHLS: Enabling Dynamic Information Flow Tracking in Hardware Accelerators," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 5, pp. 798-808, May 2019.
[doi: http://dx.doi.org/10.1109/TCAD.2018.2834421]

JR.13. C. Pilato, K. Basu, F. Regazzoni, R. Karri. "Black-Hat High-Level Synthesis: Myth or Reality?," in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 27, no. 4, pp. 913-926, April 2019.
[doi: http://dx.doi.org/10.1109/TVLSI.2018.2884742]

JR.12. C. Ciobanu, C. Pilato, G. Gaydadjiev, D. Sciuto. "The Case for Polymorphic Registers in Dataflow Computing," in *International Journal of Parallel Programming*, vol. 46, no. 6, pp. 1185–1219, December 2018.
[doi: http://dx.doi.org/10.1007/s10766-017-0494-1]

JR.11. P. Fezzardi, C. Pilato, F. Ferrandi. "Enabling Automated Bug Detection for IP-based Designs using High-Level Synthesis," in *IEEE Design & Test Magazine*, , vol. 35, no. 5, pp. 54-62, October 2018.
[doi: http://dx.doi.org/10.1109/MDAT.2018.2824121]

JR.10. C. Pilato, S. Garg, K. Wu, R. Karri, F. Regazzoni. "Securing Hardware Accelerators: a New Challenge for High-Level Synthesis," in *IEEE Embedded Systems Letter*, vol. 10, no. 3, pp. 77–80, September 2018.
[doi: http://dx.doi.org/10.1109/LES.2017.2774800]

JR.9. C. Pilato, P. Mantovani, G. Di Guglielmo, L.P. Carloni. "System-Level Optimization of Accelerator Local Memory for Heterogeneous Systems-on-Chip," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 36, no. 3, pp. 435–448, March 2017.
[doi: http://dx.doi.org/10.1109/TCAD.2016.2611506]

JR.8. R. Nane, V.-M. Sima, C. Pilato, J. Choi, B. Fort, A. Canis, Y.T. Chen, H. Hsiao, S. Brown, F, Ferrandi, J. Anderson, K. Bertels. "A Survey and Evaluation of FPGA High-Level Synthesis Tools," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 35, no. 10, pp. 1591–1604, October 2016.
[doi: http://dx.doi.org/10.1109/TCAD.2015.2513673]

JR.7. M. Lattuada, C. Pilato, F. Ferrandi. "Performance Estimation of Task Graphs based on Path Profiling," in *International Journal of Parallel Programming*, vol. 44, no. 4, pp. 735–771, August 2016.
[doi: http://dx.doi.org/10.1007/s10766-015-0372-7]

JR.6. D. Pnevmatikatos, K. Papadimitriou, T. Becker, P. Böhm, A. Brokalakis, K. Bruneel, C. Ciobanu, T. Davidson, G. Gaydadjiev, K. Heyse, W. Luk, X. Niu, I. Papaefstathiou, D. Pau, O. Pell, C. Pilato, M.D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, E. Vansteenkiste. "FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration," in *Microprocessors and Microsystems*, vol. 39, no. 4–5, pp. 321–338, June-July 2015.
[doi: http://dx.doi.org/10.1016/j.micpro.2014.09.006]

JR.5. A. Miele, C. Pilato, D. Sciuto, "A Simulation-based Framework for the Exploration of Mapping Solutions on Heterogeneous MPSoCs," in *International Journal of Embedded and Real-Time Communication Systems*, vol. 4, no. 1, pp. 22–41, April 2013.
[doi: http://dx.doi.org/10.4018/jertcs.2013010102]

JR.4. S. Cecchi, A. Primavera, F. Piazza, F. Bettarelli, E. Ciavattini, R. Toppi, J.G.F. Coutinho, W. Luk, C. Pilato, F. Ferrandi, V.M. Sima, K. Bertels, "The hArtes CarLab: A new approach to advanced algorithms development for automotive audio," in *Journal of the Audio Engineering Society*, vol. 59, no. 11, pp. 858–869, November 2011.
[url: http://www.aes.org/e-lib/browse.cfm?elib=16153]

JR.3. K. Bertels, V.M. Sima, Y. Yankova, G. Kuzmanov, W. Luk, J.G.F. Coutinho, F. Ferrandi, C. Pilato, M. Lattuada, D. Sciuto, A. Michelotti, "hArtes: Hardware-Software Codesign for Heterogeneous Multicore Platforms," in *IEEE Micro*, vol. 30, no. 5, pp. 88–97, September 2010.
[doi: http://dx.doi.org/10.1109/MM.2010.91]

JR.2. F. Ferrandi, P.L. Lanzi, C. Pilato, D. Sciuto, A. Tumeo, "Ant Colony Heuristic for Mapping and Scheduling Task and Communications on Heterogeneous Embedded Systems," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 29, no. 6, pp. 911–924, June 2010.
[doi: http://dx.doi.org/10.1109/TCAD.2010.2048354]

JR.1. C. Pilato, A. Tumeo, G. Palermo, F. Ferrandi, P.L. Lanzi, D. Sciuto, "Improving Evolutionary Exploration to Area-Time Optimization of FPGA Designs," in *Journal of Systems Architecture*, vol. 54, no. 11, pp. 1046–1057, November 2008.
[doi: http://dx.doi.org/10.1016/j.sysarc.2008.04.010]

Editorial contributions

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WS.3. M. Elhoj, A. Reis, R. Ribas, F. Ferrandi, C. Pilato, F. Moll, M. Miranda, P. Dobrovolny, N. Woolaway, A. Grasset, P. Bonnot, G. Desoli, D. Pandini, "SYNAPTIC Project: Regularity Applied to Enhance Manufacturability and Yield at Several Abstraction Levels," in *Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms* (ERDIAP 2011), Como, Italy, February 23, 2011, pp. 189-192 *(invited paper)*.
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WS.2. F. Ferrandi, M. Lattuada, C. Pilato, D. Sciuto, "Performance Estimation for Mapping and Scheduling Parallel Applications on Heterogeneous Multi-Processor Systems," in *Workshop on "The European landscape of reconfigurable computing: Lessons learned, new perspectives and innovations"* (held during DATE 2010), Dresden, Germany, March 2010, *(poster presentation)*.

WS.1. C. Pilato, F. Ferrandi, P.L. Lanzi G. Palermo, A. Tumeo, D. Sciuto, "Bambu: a High Level Synthesis Framework with Evolutionary Design Space Exploration," in *Workshop on "The New Wave of the High-Level Synthesis"* (held during DATE 2008), Munich, Germany, March 2008, *(poster presentation)*.

Teaching Experience

Doctoral level

- **Lecturer**, "Advances in System-on-Chip Design" - PhD in Information Technology (Politecnico di Milano) - 2019–2020 (*course approved*).

Graduate level

- Teaching assistant, "Digital System Design Methodologies" - Computer Engineering (Politecnico di Milano) - 2018–2019.
- Teaching collaborator, "COMS E6998: Topics in Computer Science: Embedded Scalable Platforms" - Computer Science (Columbia University) - Spring 2015, Spring 2016.
- Teaching assistant, "Progettazione Hardware" - Computer Engineering (Politecnico di Milano) - 2010–2011, 2012–2013.
- Teaching assistant, "Metodologie di Progetto Hardware" - Computer Engineering (Politecnico di Milano) - 2008–2009.

Undergraduate level

- **Lecturer**, "Informatica" - Space Engineering (Politecnico di Milano) - 2018–2019.
- **Lecturer**, "Elementi di Informatica e Reti di Calcolatori" - Communication Design (Politecnico di Milano) - 2018–2019.
- Teaching assistant, "Reti Logiche" - Online Degree on Computer Engineering (Politecnico di Milano) - 2018–2019.
- Teaching assistant, "Reti Logiche" - Computer Engineering (Politecnico di Milano) - 2007–2012, 2017–2018.
- Teaching assistant, "Architetture dei Calcolatori e Sistemi Operativi" - Telecommunications Engineering (Politecnico di Milano) - 2009–2012.
- Lab supervisor, "Informatica A" - Mathematical Engineering (Politecnico di Milano) - 2011–2012.
- Teaching assistant, "Informatica 2" - Telecommunications Engineering (Politecnico di Milano) - 2008–2009.
- Lab tutor, "Informatica 2" - Telecommunications Engineering (Politecnico di Milano) - 2007–2008.

Thesis Mentoring

- *Antonio Verlotta*, "Designing a Quantum Error Correction System on FPGA", advisor: D. Sciuto (in collaboration with the Quantum Information Science Theory Group at the National Institute of Informatics, Tokyo, Japan), 2014.

- *Matteo Mastinu*, "Design Flow to Support Dynamic Partial Reconfiguration on Maxeler Architectures", advisor: M.D. Santambrogio (in collaboration with Maxeler Technologies, London, UK, part of this thesis has been published in [IC.27] and won the "2012 HiPEAC Technology Transfer Award"), 2012.
- *Gianluca Durelli*, "A^2B: Application to Bitstream. Flusso semi automatico per lo sviluppo di MPSoC riconfigurabili", advisor: D. Sciuto, (part of this thesis has been in published in [WS.6][IC.18][IC.19]), 2012.
- *Stefano Manni*, "A Methodology for Improving the Library-Free Logic Synthesis of Integrated Circuits", advisor: F. Ferrandi, 2012.
- *Vito Giovanni Castellana* and *Silvia Lovergine*, "A Design Methodology for Efficient HLS Controllers", advisor: F. Ferrandi, (part of this thesis has been published in [IC.16]), 2010.
- *Luca Sisler*, "Metodologie di progetto per circuiti regolari", advisor: F. Ferrandi, 2010.
- *Andrea Conti*, 'Technology Mapping for Dynamic Cell Generation based on Canonical Boolean Matching", advisor: F. Ferrandi, 2009.
- *Francesca Malcotti*, "High-Level Synthesis optimization combining speculative execution and SSA-based liveness analysis", advisor: F. Ferrandi, 2008.
- *Gerardo Gallucci*, "Regularity-aware synthesis and regularity extraction from circuit RTL and structural logical representation", advisor: F. Ferrandi (in collaboration with STMicroelectronics, Agrate, MI, Italy), 2008.

In addition, Christian Pilato supervised the activity of around 20 M.Sc. and 3 Ph.D. students at Politecnico di Milano, and 2 students at Columbia University.

Academic Service

Conference and Workshop Organization

- Organizing Co-Chair for the 3rd Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Porto Conte Ricerche, September 23-27, 2019
- Organizing Co-Chair for the 2nd Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Alghero, Italy, September 17-21, 2018
- Organizing Co-Chair for the 1st Scientific School on "Designing Cyber-Physical Systems – From concepts to implementation", Porto Conte Ricerche, September 25-30, 2017
- **Program Chair** for the 12th IEEE/IFIP International Conf. on Embedded and Ubiquitous Computing (EUC 2014)
- Organizing Chair for the Workshop on "ReconfigurAble Computing for Embedded Systems" (RACES 2014), held in conjunction with the Design Automation Conference (DAC 2014)
- Program Vice-Chair and Track Chair ("Embedded System Architectures") for the 11th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC 2013)
- Organizing Co-Chair for the Workshop on "Variability modelling and mitigation techniques in current and future technologies" (VAMM 2012), held in conjunction with the conference on Design, Automation & Test in Europe (DATE 2012)

Conference and Workshop Service

- Local Arragement Chair for the ACM/IEEE International Symposium on Networks-on-Chip (NOCS 2019)
- Publicity Chair for the the 16th IFIP International Conference on Network and Parallel Computing (NPC 2019)
- Special Session and Tutorial Chair for the 37th IEEE International Conference on Computer Design (ICCD 2019)
- Publicity Chair for the ACM International Conference on Computing Frontiers (CF 2019)
- Tutorial Chair for the 36th IEEE International Conference on Computer Design (ICCD 2018)
- Special Session and Tutorial Chair for the 35th IEEE International Conference on Computer Design (ICCD 2017)
- Special Session and Tutorial Chair for the 34th IEEE International Conference on Computer Design (ICCD 2016)
- Special Session and Tutorial Chair for the 33rd IEEE International Conference on Computer Design (ICCD 2015)
- Publicity Chair for the 10th IEEE NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2015)
- Publicity Chair of the 9th IEEE International Conference on Networking, Architecture, and Storage (NAS 2014)

Technical Program Committee Work

- IEEE/ACM Design Automation Conference (DAC), 2020

- IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE), 2015–2016, 2018–2020
- HiPEAC Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RAPIDO), 2015–2020
- IEEE/ACM International Conference on Compilers, Architecture, and Synthesis of Embedded Systems (CASES), 2016–2019
- IEEE NASA/ESA Conference on Adaptive Hardware and Systems (AHS), 2015–2019
- IEEE International Conference on Field-programmable Logic and Applications (FPL), 2015–2019
- Conference on Design and Architectures for Signal and Image Processing (DASIP), 2017–2019
- IEEE/IFIP Symposium on Integrated Circuits and Systems Design (SBCCI), 2018–2019
- IEEE Southern Programmable Logic Conference (SPL), 2012–2014, 2019
- International Workshop on Top Picks in Hardware and Embedded Security, 2018
- IEEE International Conference on ReConFigurable Computing and FPGAs (ReConFig), 2012–2015, 2018
- Symposium on Parallel Computing with FPGAs (ParaFPGA), 2017
- International Workshop on Big Data Analytics (BigDAW), 2017
- International Workshop on Reliability, Security and Quality (RESCUE), 2017
- ACM International Conference on Computing Frontiers (CF), 2016–2017
- International Symposium on Applied Reconfigurable Computing (ARC), 2014–2017
- IEEE Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES), 2015–2016
- HiPEAC Workshop on Reconfigurable Computing (WRC), 2014–2016
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC), 2012–2015
- IEEE International Reconfigurable Architectures Workshop (RAW), 2013–2015
- Workshop on Variability modeling and mitigation techniques in current and future technologies (VAMM), 2012
- Workshop on Exploiting Regularity in the Design of IPs, Architectures and Platforms (ERDIAP), 2011

Editorial Experience

- Guest Editor of the special issue on "Innovative design methods for smart embedded systems" in ACM Transaction on Embedded Computing (TECS), vol. 15, no. 2, May 2016 (http://dx.doi.org/10.1145/2885505)

Reviewer Role for Conferences and Journals

- ACM Transactions on Embedded Computing (TECS)
- ACM Transactions on Architecture and Code Optimization (TACO)
- ACM Transactions on Reconfigurable Technology Systems (TRETS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Transactions on Emerging Topics in Computing
- IEEE Design & Test (D&T)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Evolutionary Computation (TEC)
- IEEE Transactions on Computers (TC)
- IEEE Embedded Systems Letters (ESL)
- Elsevier International Journal on Systems Architecture (JSA)
- International Journal of Signal Processing Systems (JSPS)
- International Journal on Microprocessors and Microsystems (MICPRO)
- International Journal of High Performance Systems Architecture (IJHPSA)
- International Journal on Design Automation for Embedded Systems (DAES)
- IEEE/ACM Design Automation Conference (DAC)
- IEEE/ACM International Conference on Design, Automation, and Test in Europe (DATE)
- IEEE International Conf. on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
- IEEE International Parallel & Distributed Processing Symposium (IPDPS)
- IEEE/ACM International Symposium on Networks-on-Chip (NOCS)
- IEEE/ACM International Conference on Embedded Software (EMSOFT)
- IEEE International Conference on Field Programmable Logic and Applications (FPL)
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM)

- IEEE International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)
- IEEE International Symposium on Circuits and Systems (ISCAS)

Memberships

- HiPEAC Member *2018 – present*
- ACM Member *2015 – present*
- IEEE and IEEE Computer Society Member *2011 – present*
- HiPEAC Affiliated Member *2008 – 2018*
- IEEE and IEEE Computer Society Student Member *2007 – 2011*

Presentations

Keynote Presentations at Conferences and Workshops

- "High-Level Synthesis: where we are and we are going" at the IEEE International Conference on Field-Programmable Technology (FPT 2017), Melbourne, Australia, December 13, 2017.
- "Bridging the Gap between Software and Hardware Designers" at the symposium on Parallel Computing with FPGAs (ParaFPGA 2017), held in conjunction with ParCo 2017, Bologna, Italy, September 12, 2017.

Invited Talks at Conferences and Workshops

- "Accelerator Memory Design for Heterogeneous System-on-Chip Architectures" at the Memory Architecture and Organization Workshop (MeAOW 2014), held in conjunction with the Embedded System Week (ESWEEK 2014), New Delhi, India, October 16, 2014.
- "Emerging challenges and trends in hardware acceleration for adaptive systems" at the Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHA'N'GE 2014), held in conjunction with the 51st Design Automation Conference (DAC 2014), San Francisco, CA, USA, June 1, 2014.
- "A2B: a Framework for the Fast Prototyping of Reconfigurable Systems" at the Workshop on Reconfigurable Computing (WRC 2013), Berlin, Germany, January 21, 2013.
- "On the Automatic Creation of Custom Standard-Cell Libraries" at the Workshop on Methods and tools to cope with the design challenges in the next generations of technologies, Milano, Italy, May 16, 2012.
- "A Design Exploration Framework for Mapping and Scheduling onto Heterogeneous MPSoCs" at the 3rd Workshop on Mapping Applications to MPSoCs, St. Goar, Germany, June 29-30, 2010.

Conference Tutorials

- "Bambu: An open-source framework for research in high-level synthesis" at the IEEE International Conference on Field-Programmable Technology (FPT 2017), Melbourne, Australia, December 14, 2017.
- "Designing Multi-Bank Memories for Heterogeneous Architectures" at the ACM/IEEE Embedded Systems Week (ESWEEK 2017), Seoul, South Korea, October 15, 2017.
- "Bambu: An open-source framework for research in high-level synthesis" at the IEEE International Conference on Field-Programmable Logic and Applications (FPL 2017), Ghent, Belgium, September 7, 2017.

Academic Seminars

- "Hardware security and high-level synthesis: the good, the bad and the ugly" at Columbia University, New York, NY, USA, November 9, 2018.
- "Optimizing private local memories in heterogeneous architectures" at University of California Irvine (UCI), Irvine, CA, USA, June 14, 2017.
- "Designing and Optimizing Hardware Accelerators with Private Local Memories" at Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, May 24, 2017.
- "TaintHLS: Enabling Dynamic Information Flow Tracking in Hardware Accelerators" at New York University (NYU), New York, NY, USA, November 2, 2016.
- "System-Level Memory Optimization for Heterogeneous System-on-Chip Architectures" at Università della Svizzera italiana (USI), Lugano, Switzerland, January 16, 2015.
- "Design Challenges and Techniques for Heterogeneous Reconfigurable Systems" at École Polytechnique, Montréal, QC, Canada, September 26, 2013.

- "On the Automatic Synthesis of Hardware Accelerators for Improving Embedded Systems" at Columbia University, New York, NY, USA, May 23, 2013.
- "Accelerating research in reconfigurable computing: the FASTER approach" at Massachusetts Institute of Technology (MIT), Boston, MA, USA, May 22, 2013.

Industrial Seminars

- "PandA-Bambu: A free software framework for the High-Level Synthesis of Complex Applications" at European Space Research and Technology Centre (ESA-ESTEC), Noordwijk, The Netherlands, April 12, 2012.
- "Field Programmable Gate Array (FPGA): design and testability" at Alenia AerMacchi, Venegono Inferiore (VA), Italy, February 3, 2008.

References

- Donatella Sciuto, Professor and Vice Rector
  Dip. di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy
  Tel: +39 02-2399-3662 – Email: donatella.sciuto@polimi.it
- Luca P. Carloni, Professor
  Department of Computer Science, Columbia University, New York, USA
  Tel: +1 (212) 939-7043 – Email: luca@cs.columbia.edu
- Ramesh Karri, Professor and Co-Founder of the NYU Center for Cybersecurity
  Department of Electrical and Computer Engineering, New York University, New York, USA
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Milano, September 21, 2019

Signature

Christian Pilato