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Born: July 10, 1973—Naples, Italy
Nationality: Italian

International scientific achievements

H-index	**10**[1]
Books	**1** book and **2** international book chapters.
Journals	**10** journal papers published and/or accepted for publication, of which **4** IEEE or ACM Transactions.
Conference	**28** conference and symposia papers published and/or accepted for publication.
Workshops	**10** published and/or presented works in international workshops.
Patents	**2** EU patents and **2** US patents.

Education

2002	Ph.D. in Computer Engineering (*Dottorato di Ricerca in Ingegneria Informatica e Automatica*), Politecnico di Milano, Italy
1998	Ms. in Computer Engineering (*Laurea in Ingegneria Informatica*), Politecnico di Milano, Italy

Current position

Assistant Professor (tenure-track), Politecnico di Milano, Italy

Areas of specialization

Computer aided design of digital circuits with emphasis on multi-processor design space exploration and network-on-chip design, low-power and high-performance design of parallel

[1] Index suggested by Jorge E. Hirsch (UCSD) as a tool for determining the research *quality*. H-index $= h$ if h of N_p publications have at least h citations and the other $(N_p - h)$ papers have at most h citations each. The H-index has been computed with Google Scholar (http://scholar.google.com) on January 4th, 2009.

processor architectures and advanced parallel programming paradigms, compilation and simulation methodologies for multi-processor-based systems.

Appointments held

2011-today *Assistant Professor* (tenure-track), Politecnico di Milano, Italy

- Involved in the technical management of the European Project FP7 titled "PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures" (2PARMA).
- Investigating techniques for advanced design space exploration of many-core architectures, response-surface modelling, run-time management, parallel programming models, virtual platform design, audio processing.
- Leading research and development activities for MOST, an advanced tool for design space exploration.

2009-2011 *Assistant Professor* (without tenure), Politecnico di Milano, Italy

- Involved in the technical management of the European Project FP7 titled "PARallel PAradigms and Run-time MAnagement techniques for Many-core Architectures" (2PARMA).
- Involved in the management of the European Project FP7 titled "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (MULTICUBE).
- Introducing advanced techniques for managing run-time variability in automatic design space exploration for multi-processors.
- Leading research and development activities for Multicube Explorer, a tool for design space exploration (open-source since 2009).

2007-2009 *Research Associate*, Politecnico di Milano, Italy

- Involved in the management of the European Project FP7 titled "Multi-objective design space exploration of multi-processor SoC architectures for embedded multimedia applications" (MULTICUBE).
- Introduced advanced techniques for managing design of experiments and response surface methods in automatic design space exploration for multi-processors.
- Extended classical design space exploration to tackle the problem of process-variability-aware design of multi-processors.
- Leading research and development activities for Multicube Explorer, an advanced tool for design space exploration (open-source since 2009).
- Leading research and development activities on the *stream programming* paradigm with applications to advanced, parallel architectures such as the IBM Cell and multi-core x86 processors.

2004-2007 *R&D Engineer*, STMicroelectronics, Switzerland.

- Architectural specification and development of ST200 processors, including symmetric multi-processing, virtualization and secure storage.
- Development of extensions to industrial network-on-chip architectures.
- Development of the simulation platform infrastructure for the ST200 processor family and streaming architectures.
- Benchmarking of streaming and multi-processor architectures.

2003-2004 *Research Consultant*, STMicroelectronics, Milan.

- High-level modeling and characterization of power consumption of industrial networks-on-chip, among which AMBA and STBUS.
- Development of tools and methodologies for supporting industrial, low-power STBUS network-on-chip.

2002-2002 *Post-Doc Researcher*, Politecnico di Milano

- Investigated power estimation at the system level for systems-on-chip.
- Investigated design space power/performance exploration at the system level for systems-on-chip.

1999-2002 *Ph.D. Candidate*, Politecnico di Milano

- Developed an analytical, micro-processor power consumption model for VLIW architectures.
- Successfully modeled the instruction-level energy consumption of the ST200 processors, jointly designed by HPLabs and STMicroelectronics.
- Defined innovative register file write inhibition schemes that exploit the forwarding paths in VLIW processors for reducing power.
- Specified and implemented novel dynamic power management policies for general purpose operating systems.
- Defined a design exploration framework to enable an efficient fine-tuning of the configurable modules of an embedded system.