

CURRICULUM VITÆ

MARCO D. SANTAMBROGIO

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1 PERSONAL DATA

1.1 General data

Name Marco Domenico

Surname Santambrogio

Date of birth November 4, 1977

Place of birth Monza (MB) - Italy

Citizenship Italian

Marital status Married

Office @ PoliMi Dipartimento di Elettronica e Informazione
Politecnico di Milano
Via G. Ponzio 34/5
Milano, Italy 20133

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1.2 Publications

- SCOPUS Author ID: 11540913800 - <https://www.scopus.com/authid/detail.uri?authorId=11540913800> [h-index: 25 @ July 2022]
- ORCID: 0000-0002-9883-9693 - <https://orcid.org/0000-0002-9883-9693>
- Google Scholar: <https://scholar.google.com/citations?user=Dr2SsKIAAAAJ> [h-index: 37, i10-index: 123 @ July 2022]
- DBLP: http://dblp.uni-trier.de/pers/hd/s/Santambrogio:Marco_D=.html
- Research Gate: https://www.researchgate.net/profile/Marco_Santambrogio

1.3 Academic positions and affiliations

- Academic positions

Since 2/2018 Associate Professor at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

Since 2/2011 Assistant Professor (with tenure) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

Since 12/2009 Adjunct Professor in the College of Engineering of University of Illinois at Chicago (Chicago, Illinois, USA).

03/2010 - 02/2014 Research Affiliate at Massachusetts Institute of Technology - Computer Science and Artificial Intelligence Laboratory (Cambridge, MA - USA).

11/2009 - 1/2011 Postdoc/Research Assistant at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

02/2009 - 02/2010 Postdoc Fellow (research : Self-Aware Computing Systems.) at Massachusetts Institute of Technology - Computer Science and Artificial Intelligence Laboratory (Cambridge, MA - USA).

07/2008 - 10/2009 Research Assistant (research program: Metodologie di progetto di sistemi informatici hardware e software. (Design methodologies for hardware and software IT systems.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

- 03/2008-07/2008** Research Assistant (research program: Analisi e definizione di possibili scenari applicativi di nuovi sistemi riconfigurabili. (Analysis and definition of applicative scenarios for novel reconfigurable technologies.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 03/2005-02/2008** PhD Student in the Computer Engineering and Automation program at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).
- 11/2004-03/2005** Research Assistant (research program: Definizione di un flusso di design per sistemi riconfigurabili basati su FPGA della Xilinx. (Definition of a novel design flow for Xilinx FPGA-based reconfigurable systems.)) at the Dipartimento di Elettronica ed Informazione of Politecnico di Milano (Milano, Italy).

- Affiliations

- Since 2013** Senior Member of the Association for Computing Machinery (ACM)
- Since 2011** Senior Member of the Institute of Electrical and Electronic Engineers (IEEE)
- Since 2009** Member of the Italian Scientists and Scholars of North America Foundation (ISSNAF)
- Since 2008** Member of HiPEAC Reconfigurable Computing Cluster
- Since 2008** Member of HipEAC, European Network of Excellence on High Performance and Embedded Architecture and Compilation
- Since 2008** Member of the Association for Computing Machinery (ACM)
- Since 2008** Member of the IEEE Circuits and Systems Society (CAS)
- Since 2008** Member of the IEEE Computer Society (CS)
- Since 2005** Member of the Institute of Electrical and Electronic Engineers (IEEE)

1.4 Education

- 15 May, 2008 PhD in Information Engineering**
 DIPARTIMENTO DI ELETTRONICA ED INFORMAZIONE, POLITECNICO DI MILANO
 PhD Thesis: *Hardware/Software codesign methodologies for dynamically reconfigurable systems.*
 Advisor: Prof. D. Sciuto. Tutor: Prof. F. Ferrandi
- June 2004 Master of Science in Computer Science**
 UNIVERSITY OF ILLINOIS AT CHICAGO, CHICAGO, ILLINOIS, USA
 Master Thesis: *Dynamic Reconfigurability in Embedded System Design. A Model for the Dynamic Reconfiguration.*
 Advisor: Prof. John Lillis.
- April 2004 Laurea (MSc equivalent) in Computer Engineering**
 POLITECNICO DI MILANO
 Thesis: *A Methodology for Dynamic Reconfigurability in Embedded System Design.*
 Advisor: Prof. D. Sciuto.

1.5 Visiting periods

- Postdoc Fellow, Massachusetts Institute of Technology, February 2009 - February 2010
- Visiting researcher, Heinz Nixdorf Institute, January 2009
- Invited researcher, Northwestern University, April - May 2007
- Invited researcher, Northwestern University, February - June 2006
- Visiting researcher, Heinz Nixdorf Institute, January 2006
- MSc Student, University of Illinois at Chicago, 2002

1.6 Service Activities

- @ Politecnico di Milano

Since Sept 2019 Politecnico di Milano Director for the PoliMi-UIC Double Degree Program

Since May 2019 Computer Eng. Coordinator for the PoliMi-UIC Double Degree Program

Since 2017 Member of the organizing committee of the *Innovation in Teaching Activities Initiative* for DEIB

2013 - 2015 Member of the organizing committee of the OpenHouse event (Information Technology Section)

Since 2012 NECSTLab Founder and Director

2010 - 2012 MicroLAB Director

Since 2011 Founder and head of the Rocca Fellows community

Since 2010 Organizer of the OpenDay event on behalf of the DEIB Information Technology Section

2008 - 2012 Founder and head of the PhDEI *Association*.

07/2005 - 12/2006 Head of the ICT area and member of the managing board of ISF-MI Association.

July 2005 Co-founder of Engineer Without Border Milano (Ingegneria Senza Frontiere ISF-MI).

- @ Others

Since Nov 2019 Chair of the IEEE Italian Chapter of the Computer Society

Since 2016 Member of the IEEE CS Member & Geographic Activities Board

Since 2016 Chair of the IEEE CS ARC Larson Paper Prize

2015 - 2019 Vice-Chair of the IEEE Italian Chapter of the Computer Society

Since 2013 Member of the IEEE Italy Section as Student Activities Coordinator.

2012 - 2015 Member of the IEEE CS Student Awards Committee (SAC).

Since 2012 Member of the IEEE CS Awards and Recognition Committee (ARC) - <https://www.computer.org/web/chapters/mga-board>

2009 - 2012 Member of the MIT Postdoctoral Advisory Council.

2009 - 2012 Member of the National Postdoctoral Association (NAP).

01/2009 Co-founder and president of the iDRESA Association.

01/2001- 04/2001 Head of the IT area, for Caritas Ambrosiana and CeLIM, of two humanitarian missions in Kosovo (Jacova e Pristina)

02/2000 - 12/2000 Civil service at CeLIM NGO.

2 SCIENTIFIC ACTIVITIES

2.1 International Conferences and Journal Organization

2.1.1 Journal Editorial Activities

- **Editorial advisory board members:**

- Title: IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)
Editor: IEEE
References: <https://www.computer.org/csdl/journal/td>
From: Sept, 2018
- Title: Elsevier Editorial Board of Big Data Research, Editor of the area Cyber-Physical Systems
Editor: Elsevier
References: <http://www.journals.elsevier.com/big-data-research/editorial-board/>
From: Dec 17, 2013

- **Journal Special Issue Editor**

- ACM Transactions on Reconfigurable Technology and Systems - Special section on the 22nd Reconfigurable Architectures Workshop (RAW 2014)
- ACM Transactions on Reconfigurable Technology and Systems - Special section on the 10th International Symposium on Reconfigurable Computing: Architectures, Tools, and Applications (ARC 2014)
- Elsevier Journal on Future Generation Computer Systems (FGCS) - Special issue on the 10th International Conference on Embedded and Ubiquitous Computing (EUC 2012) (special session title: Multicore and Many-core Architectures for Future Generation Embedded)

- **Journal Guest Editor**

- Microprocessor and Microsystems Journal, Special Issue
Title: Embedded Multicore Systems: Architecture, Performance and Application.
Editor: Elsevier
Guest editors: M. Chang, P.A. Hsiung, M. D. Santambrogio, W. H. Lee
References: http://www.elsevier.com/locate/jmcs/cfp/Call_for_papers_Multicore_Embedded.pdf
- EURASIP Journal of Reconfigurable Computing
Title: Self-Awareness in Reconfigurable Computing Systems.
Editor: Hindawi Publishing Corporation
Guest editors: T. Becker, M. D. Santambrogio, M. Happe, M. Platzner,
References: <http://www.hindawi.com/journals/ijrc/si/807910/cfp/>
- International Journal on Reconfigurable Computing, Special Issue
Title: Selected Papers from the International Conference on Reconfigurable Computing and FPGAs (ReConFig'10)
Editor: Hindawi Publishing Corporation
- Journal of Systems Architecture
Title: Design Flows and System Architectures for Adaptive Computing on Reconfigurable Platforms.
Editor: Elsevier
Guest editors: M. D. Santambrogio, I. Bravo
References: <http://www.elsevier.com/inca/publications/misc/JSASI-AdaptiveComputingTrends.pdf>
- EURASIP Journal on Embedded Systems
Title: Reconfigurable computing and hardware/software codesign.
Editor: Hindawi Publishing Corporation
Guest editors: T. Plaks, M. D. Santambrogio, D. Sciuto
References: www.hindawi.com/journals/es/si/rcc.pdf
www.hindawi.com/journals/es/raa.731830.html

2.2 Program committee, conference organization and revision activities

2.2.1 Steering Committee

- IEEE International Conference on Cyber, Physical and Social Computing (CPSCoM): 2017
- Embedded Operating System Workshop (EWiLi): 2016, 2017
- IEEE International Conference on Networking, Architecture, and Storage (NAS): 2014, 2015

2.2.2 General Chair

- Annual IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP): 2018
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC): 2014
- IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA): 2014
- IEEE International Conference on Cyber, Physical and Social Computing (CPSCoM): 2013

2.2.3 Program Chair

- IEEE International Conference on Field Programmable Logic and Applications (FPL): 2010 (226 submitted papers, 60 regular papers), 2017
- IEEE International Conference on Smart City (SmartCity): 2016
- IEEE Reconfigurable Architectures Workshop (RAW): 2014, and 2015
- IEEE International Conference on Cyber, Physical and Social Computing (CPSCoM): 2015
- International Symposium on Applied Reconfigurable Computing (ARC): 2014
- HiPEAC Workshop on Reconfigurable Computing (WRC): 2014
- IEEE International Conference on Networking, Architecture, and Storage (NAS): 2013
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC): 2012

2.2.4 Program Vice-Chair

- IEEE Reconfigurable Architectures Workshop (RAW): 2013
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC) - Embedded Systems and Hardware/Software Co-Design: 2011

2.2.5 Topic Chair

- Topic Chair for the topic A6: Reliable and Reconfigurable Systems in Design, Automation & Test in Europe (DATE): 2015

2.2.6 Topic Co-Chair

- Topic Co-Chair for the topic A6: Reliable and Reconfigurable Systems in Design, Automation & Test in Europe (DATE): 2012, 2013, and 2014

2.2.7 Track Chair

- IEEE International Conference on Field Programmable Logic and Applications (FPL): 2013, and 2021

2.2.8 Workshop Organizer

- IEEE Reconfigurable Architectures Workshop (RAW): 2016, 2017, 2018, 2019, 2020, 2021, and 2022
- FPL Workshop on Reconfigurable Computing for Machine Learning: 2019, 2020, 2021, and 2022
- International Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE): 2011, 2012, 2013, 2014, 2015, and 2016
- International Conference on Industrial and Information System: 2007

2.2.9 Program Committee

- Design Automation Conference (DAC): 2012, 2013, 2014, 2020, 2021, and 2022
- Design, Automation & Test in Europe (DATE): 2012, 2013, 2014, 2015, 2016, 2019, 2020, 2021, and 2022
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM): 2013, 2014, 2015, 2016, 2017, 2018, 2020, 2021, and 2022
- Conference on Hardware/Software CoDesign and System Synthesis (CODES-ISSS): 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, and 2022
- IEEE International Conference on Field Programmable Logic and Applications (FPL): 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2021, and 2022
- IEEE Reconfigurable Architectures Workshop (RAW): 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021, and 2022
- ACM International Conference on Supercomputing (ICS): 2020, and 2022
- ACM Great Lakes Symposium on VLSI (GLSVLSI): 2019, 2020, 2021, and 2022
- IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MC-SoC): 2015, 2017, 2019, 2020, and 2021
- International Conference on High Performance Computing & Simulation (HPCS): 2020
- IEEE International Conference on Computer Design (ICCD): 2020
- International Symposium on Applied Reconfigurable Computing (ARC): 2015, 2016, 2017, 2018, 2019, and 2020
- International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC): 2016, and 2020
- International Conference on Computer-Aided Design (ICCAD): 2015, 2016, 2017, and 2019
- Southern Conference on Programmable Logic (SPL) Conference: 2008, 2009, 2010, 2011, 2012, and 2019
- NASA/ESA Conference on Adaptive Hardware and Systems (AHS): 2012, 2013, 2014, 2015, 2017, 2018, and 2019
- International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS): 2015, 2016, 2017, 2018
- International Conference on ReConFigurable Computing and FPGAs (ReConFig): 2006, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, and 2018
- IEEE International Symposium on Parallel and Distributed Processing with Applications (ISPA): 2015, 2016, 2017, and 2018
- ACM International Conference on Computing Frontiers (CF): 2016, and 2017

- IEEE International Conference on Cloud and Autonomic Computing (ICCAC): 2015, 2016, and 2017
- International Workshop on Reconfigurable Communication-centric Systems-on-Chip (Re-CoSoC): 2012, 2013, 2014, 2015, and 2016
- Workshop on Reconfigurable Computing (WRC): 2010, 2011, 2012, 2013, 2014, 2015, and 2016
- International Workshop on Highly Efficient Accelerators and Reconfigurable Technologies (HEART): 2010, and 2016
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing: 2009, 2010, 2011, 2012, 2013, 2014, and 2015
- Embedded Operating System Workshop (EWiLi): 2013, 2014, and 2015
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC): 2014
- International Workshop on Adaptive and Reconfigurable Embedded Systems (APRES): 2014
- International Workshop on Reconfigurable Architectures and Self-adaptive Autonomic Systems (RASAS): 2014
- International Workshop on Multi-Objective Many-Core Design (MOMAC): 2014
- IEEE International Conference on Emerging Technologies & Factory Automation (ETFa): 2014
- Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES): 2014
- IEEE International Conference on Networking, Architecture, and Storage (NAS): 2010, 2011, 2012, and 2013
- International Symposium on System-on-Chip (SoC): 2009, 2010, 2011, 2012, and 2013
- International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA) Conference: 2006, 2007, 2008, 2009, 2010, 2011, and 2012
- International Workshop on Mobile Computing in the Clouds (MobiCloud): 2013
- IEEE International Symposium on Embedded Multicore SoCs (MCSoc): 2013
- IEEE Real-Time and Embedded Technology and Applications Symposium, RTAS (Applied Methodologies and Foundations): 2012
- European Conference on the Applications of Evolutionary Computation (EVO): 2011
- IEEE Field Programmable Technology (FPT): 2007, 2008, 2009, and 2010
- SPIE Conference: Microtechnologies for the New Millennium 2009 and 2010
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI): 2009 and 2010
- International Workshop on Reconfigurable and Multicore Embedded Systems (WoRMES): 2009

2.2.10 National Workshops and Seminars Organization

- Scientific board member *CALL4BRAIN* - <http://www.call4brain.com/>, TEDMED, De Donato - Politecnico di Milano, Milano, Dec. 2, 2016.
- *Reconfigurable Computing Italian Workshop*, first Italian Meeting, S01 - Politecnico di Milano, Milano, Dec. 19, 2008.
- *Partial Dynamic Reconfiguration Workshop*, Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
- *IEEE Expert now: Tutorial on-line*, IEEE Delegation, DEI - Politecnico di Milano, September 2007.

2.2.11 Revision activities

- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- IEEE Transaction on Computer-Aided Design (TCAD)
- IEEE Transaction on Computer (TOC)
- IEEE Micro
- IEEE Transactions on Industrial Informatics (TII)
- IEEE Transaction on Evolutionary Computation
- IEEE Embedded Systems Letters (ESL)
- IEEE Transactions on Signal Processing
- ACM Computing Reviews
- ACM Transaction on Reconfigurable Technology and Systems (TRETs)
- ACM Transactions on Embedded Computing Systems (TECS)
- Design Automation for Embedded Systems (DAEM)
- Journal of Systems Architecture (JSA) - Elsevier
- Integration, the VLSI Journal - Elsevier
- Computers & Electrical Engineering - Elsevier
- International Journal of Circuit Theory and Applications (IJCTA) - Wiley
- Journal of Computer Science and Technology (JCST)
- International Conferences:
 - Design Automation Conference (DAC);
 - International Conference on Computer-Aided Design (ICCAD);
 - IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM);
 - Design, Automation and Test in Europe (DATE);
 - IEEE International Symposium on Circuits and Systems (ISCAS);
 - IEEE International Conference on Field Programmable Logic and Applications (FPL);
 - IEEE Reconfigurable Architectures Workshop (RAW);
 - IEEE Computer Society Annual Symposium on VLSI (ISVLSI);
 - IEEE International Conference on Field-Programmable Technology (FPT);
 - ACM Great Lakes Symposium on VLSI (GLSVLSI);
 - IEEE/IFIP International Conference on Embedded and Ubiquitous Computing;
 - International Workshop on Reconfigurable and Multicore Embedded Systems (WoRMES);
 - IFIP International Conference on Very Large Scale Integration (VLSI-SoC);
 - International Symposium on System-on-Chip (ISSoC);
 - Southern Conference on Programmable Logic (SPL) Conference;
 - Engineering of Reconfigurable Systems and Algorithms (ERSA);
 - International Conference on Green Circuits and Systems (ICGCS).

2.3 Invited talks and Panelists

- Invited talks

- *The NECSTCamp Project*
Speaker: M. D. Santambrogio.
, Northwestern University, Evanston, IL, USA, 5 May, 2022.
- *The NECSTCamp Project*
Speaker: M. D. Santambrogio.
, University of Illinois at Chicago, Chicago, IL, USA, 2 May, 2022.
- *The NECSTLab Multi-Faceted Experience with AWS F1 - Teaching, Research Framework and Application stack - Keynote Speech*
Speaker: M. D. Santambrogio
HiPEAC Workshop on Reconfigurable Computing (WRC), Valencia, Spain, 21 Jan, 2019.
- *NECSTLab: Research and Innovation.*
Speaker: M. D. Santambrogio.
, Totemic, Palo Alto CA, USA, 29 May, 2019
- *The NECSTLab experience on teaching FPGAs via MOOCs and live classes!.*
Speaker: M. D. Santambrogio.
, Xilinx, San Jose, CA, USA, 24 May, 2019
- *NECSTLab: Research and Innovation.*
Speaker: M. D. Santambrogio.
, Intel, Santa Clara, CA, USA, 24 May 2019
- *NECSTLan @ a Glance.*
Speaker: M. D. Santambrogio.
, Oracle Labs, Redwood Shores, CA, USA, 22 May, 2019
- *NECSTLan @ a Glance.*
Speaker: M. D. Santambrogio.
, Open Network Foundation, Menlo Park, CA, USA, 21 May 2019
- *NECSTLab: uno sguardo sul futuro.*
Speaker: M. D. Santambrogio.
E-Novia FlashForward, Milano, 2019
- *The NECSTLab Multi-Faceted Experience with AWS F1 - Teaching, Research Framework and Application stack.*
Speaker: M. D. Santambrogio.
Amazon AWSome Day Milano, Talent Garden, Milano, Settembre, 2018
- *Innovative Learning Initiative: Rationality and on how to collaborate.*
Speaker: M. D. Santambrogio.
Stanford University, Center to Support Excellence in Teaching, Stanford, CA, USA, 29 May, 2018
- *The NECSTLab Multi-Faceted Experience with AWS F1.*
Speaker: M. D. Santambrogio, Lorenzo Di Tucci, Marco Rabozzi.
Xilinx, San Jose, CA, USA, 25 May, 2018
- *NECSTLab and Microsoft.*
Speaker: M. D. Santambrogio.
Microsoft, Mountain View, CA, USA, 7 June, 2017
- *NECST at a Glance and the DReAMS Research Line.*
Speaker: M. D. Santambrogio.
Xilinx, San Jose, CA, USA, 8 June, 2017
- *Heterogeneous exascale Supercomputing: the Role of CAD in the exaFPGA Project.*
Speaker: M. D. Santambrogio.
Design, Automation & Test in Europa, Talk in a special session at DATE 17, Lausanne, Switzerland, 28 March, 2017
- *NECST and Xilinx: an interesting history.*
Speaker: M. D. Santambrogio.
Xilinx, San Jose, CA, USA, 2 June, 2016

- *The NECST experience.*
Speaker: M. D. Santambrogio.
Oracle Labs, Redwood Shores, CA, USA, 1 June, 2016
- *A self-adaptive approach to efficiently manage energy and performance in tomorrow's heterogeneous computing systems.*
Speaker: M. D. Santambrogio.
Design, Automation & Test in Europa, Talk in an special session at DATE 16, Dresden, Germany, 16 March, 2016
- *Operating System-Level Performance and Power Management: from Datacenters to Embedded Systems.*
Speaker: M. D. Santambrogio.
The International Conference on Hardware-Software Codesign and System Synthesis, CODES+ISSS 15, Amsterdam, Dutch, 6 October, 2015
- *A bird's eye view on the NECST Lab: What (i/wa)s the DRES D project.*
Speaker: M. D. Santambrogio.
Xilinx, San Jose, CA, USA, 10 June, 2015
- *On how to implement efficient mobile devices power modelling, and design methodologies for smart spaces.*
Speaker: M. D. Santambrogio.
Samsung Research America, Mountain View, CA, USA, 9 June, 2015
- *From FPGA-based Reconfigurable Systems to Autonomic Adaptive Computing Systems an Enabling Technologies Perspective.*
Speaker: M. D. Santambrogio
Stanford University, Stanford, CA, USA, 6 June, 2014
- *Cores Allocation and Relocation Management for Self Dynamic Reconfigurable Systems.*
Speaker: M. D. Santambrogio
ALTERA, San Jose, CA, USA, 5 June, 2014
- *A bird's eye view on the NECST Lab and behind the scene of this meeting.*
Speaker: M. D. Santambrogio
Berkeley, CA, USA, 2 June, 2014
- *How to enable FPGA-based self-adaptive computing systems - Keynote Speech*
Speaker: M. D. Santambrogio
Workshop co-located with FPL 2013 entitled "Challenges of Embedded Robotics. Can FPGAs Overcome Them?", Porto, Portugal, 6 September, 2013.
- *A bird's eye view on the NECST Lab and behind the scene of this meeting.*
Speaker: M. D. Santambrogio.
MIT, MA, USA, 22 May, 2013
- *The Autonomic Operating System Research Project - Achievements and Future Directions.*
Speaker: M. D. Santambrogio.
Design Automation Conference, DAC 2013, Austin, Texas, June 2 - 6, 2013
- *The CHANGE project: Enabling Technologies For Self-Aware Adaptive Computing Systems.*
Invited Speaker: M. D. Santambrogio.
Workshop on Self-Awareness in Reconfigurable Computing Systems (SRCS), Oslo, Norway, September 1, 2012
- *The CHANGE project: Enabling Technologies For Self-Aware Adaptive Computing Systems.*
Speaker: M. D. Santambrogio and F. Sironi.
IBM Research, Austin, TX, USA, 9 August, 2012
- *The CHANGE project: Enabling Technologies For Self-Aware Adaptive Computing Systems.*
Speaker: M. D. Santambrogio and F. Sironi.
Oracle, Belmont, CA, USA, 8 June, 2012

- *The CHANGE project: Enabling Technologies For Self-Aware Adaptive Computing Systems.*
Speaker: M. D. Santambrogio and F. Sironi.
Yahoo, Santa Clara, CA, USA, 4 June, 2012
- *The CHANGE project: Enabling Technologies For Self-Aware Adaptive Computing Systems.*
Speaker: M. D. Santambrogio.
University of Illinois at Chicago, Chicago, IL, USA, September 15, 2011
- *The CHANGE project: Enabling Technologies For Self-Aware Adaptive Computing Systems.*
Speaker: M. D. Santambrogio.
GDR SOC-SIP, Systemes multiprocesseurs : outil, modele pour l'estimation de la consommation, techniques d'optimisation, Paris, France, March 21, 2011
- *Enabling Technologies For Self-Aware Adaptive Systems.*
M. D. Santambrogio, H. Hoffmann, J. Eastep, J. E. Miller, A. Agarwal.
NASA/ESA Conference on Adaptive Hardware and Systems, AHS 2010, Anaheim California, USA, June 15 - 18, 2010
- *From Reconfigurable Architectures to Self-Adaptive Autonomic Systems.* - Keynote Speech
Speaker: M. D. Santambrogio
International Workshop on Reconfigurable and Multicore Embedded System, August 29, 2009.
- *A parallel-serial decimal multiplier architecture.*
L. Dadda, M. D. Santambrogio
4th Logic Synthesis Italian Day, Politecnico di Milano, Milano, June 30, 2008.
- *Reconfiguration technologies and DRES contribution.*
Speaker: M. D. Santambrogio
Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
- *Design Flow for System-on-Programmable Chip.*
Speaker: M. D. Santambrogio
Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
- *Partial Dynamic Reconfiguration: Real Needs and Limits.*
Speaker: M. D. Santambrogio
Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
- *Partial Dynamic Reconfiguration: Basic Concepts.*
Speaker: M. D. Santambrogio
Nokia Siemens Networks, Cinisello Balsamo, Milano, April 23, 2008.
- *Dynamic Reconfigurability in Embedded System Design.*
Speaker: M. D. Santambrogio
Heinz Nixdorf Institute, Paderborn, Germany, January 26, 2006.

- **Panelist**

- April 24 - 15, 2012, Goteborg, Sweden, HiPEAC Computing Systems Week April 2012, *Design and runtime management of reconfigurable systems*
- July 9 - 11, 2012, York, UK, 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), *Maturity of high level synthesis tools - useful or just another hype?*

3 TEACHING ACTIVITIES CARRIED OUT IN ITALIAN OR FOREIGN UNIVERSITIES OR BODIES

3.1 Courses with a primary responsibility

- Coursera
 - Course: FPGA computing systems: Background knowledge and introductory materials
<https://www.coursera.org/learn/fpga-intro>
Teacher: prof. M. D. Santambrogio
Graded: 4.6/5
Available online since: April 2018
 - Course: Developing FPGA-accelerated cloud applications with SDAccel: Theory
<https://www.coursera.org/learn/fpga-sdaccel-theory>
Teacher: prof. M. D. Santambrogio
Graded: 4.8/5
Available online since: April 2019
 - Course: Developing FPGA-accelerated cloud applications with SDAccel: Practice
<https://www.coursera.org/learn/fpga-sdaccel-practice>
Teacher: prof. M. D. Santambrogio
Graded: 4.3/5
Available online since: May 2019
- University: Politecnico di Milano (Milano, Italy):
 - **PhD Course**
 - * Course: Advanced Topic on Reconfigurable FPGA-Based Systems Design
Teacher: prof. M. D. Santambrogio, prof. A. R. Miele
Academic Year: 18/19, 16/17
 - * Course: Advanced Topics on Heterogeneous System Architectures: architectures, programming models and resource management
Teacher: prof. M. D. Santambrogio, prof. A. R. Miele
Academic Year: 20/21, 17/18
 - * Course: FPGA-Based Systems Design
Teacher: prof. M. D. Santambrogio
Academic Year: 13/14
 - * Course: Parallelism in Wonderland; are you ready to see how deep the rabbit hole goes?
Teachers: prof. M. D. Santambrogio, prof. S. Campanoni
Academic Year: 13/14
 - * Course: From Reconfigurable Hardware to Self-Adaptive Computer Architectures
Teacher: prof. M. D. Santambrogio
Academic Year: 13/14, 12/13
 - **Master Degree**
 - * Course: Advanced Computer Architecture - Graduate Course
Teachers: prof. M. D. Santambrogio
Academic Year: 21/22, 20/21, 19/20
 - * Course: High Performance and Processors and Systems - Graduate Course
Teachers: prof. M. D. Santambrogio
Academic Year: 21/22, 20/21, 19/20
 - **Undergraduate Course**
 - * Course: Informatica ed Elementi di Informatica Medica - (Bio Eng students)
Teacher: prof. M. D. Santambrogio
Academic Year: 21/22, 20/21, 19/20, 18/19, 17/18, 16/17, 15/16, 14/15, 13/14, 12/13, 11/12
 - * Course: Informatica B - (Mech Eng studentes)
Teacher: prof. M. D. Santambrogio
Academic Year: 21/22, 20/21, 19/20, 18/19, 17/18, 16/17, 15/16, 14/15, 13/14, 10/11

* Course: Projects of Ingegneria Informatica - Undergraduate Course
Teacher: prof. M. D. Santambrogio
Academic Year: 09/10, 08/09

- University: University of Illinois at Chicago (Chicago, Illinois - USA):
 - Course: Advanced Computer Architecture (CS/ECE/MENG 466) - Graduate Course (taught in English)
Teacher: prof. M. D. Santambrogio
Academic Year: 17/18, 13/14, 11/12, 10/11, 09/10

3.2 Teaching Assistantships

- University: Politecnico di Milano (Milano, Italy):
 - Course: Architettura Avanzata dei Calcolatori (Advanced Computer Architecture) - Graduate Course
Teacher: prof. D. Sciuto
Academic Year: 18/19/ 17/18, 16/17, 15/16, 14/15, 10/11
 - Course: High Performance and Processors and Systems - Graduate course (taught in English)
Teacher: prof. D. Sciuto
Academic Year: 18/19/ 17/18, 16/17, 15/16, 14/15, 13/14, 12/13, 11/12, 10/11, 09/10, 07/08, 06/07
 - Course: Architettura Avanzata dei Calcolatori (Advanced Computer Architecture) - Graduate Course
Teacher: prof. R. Negrini
Academic Year: 12/13, 11/12
 - Course: Architettura dei Calcolatori (Computer Architecture) - Graduate Course
Teacher: prof. D. Sciuto
Academic Year: 08/09, 07/08, 06/07
 - Course: Reti Logiche A - Undergraduate Course
Teacher: prof. C. Bolchini
Academic Year: 08/09, 07/08, 06/07, 05/06, 04/05
 - Course: Reti Logiche B - Undergraduate Course
Teacher: prof. F. Salice
Academic Year: 05/06
 - Course: Informatica I - Undergraduate Course
Teacher: prof. C. Bolchini
Academic Year: 05/06
- University: Advanced Learning and Research Institute, master in Embedded Systems (Lugano, Switzerland):
 - Course: Design Technologies - Graduate course (taught in English)
Teacher: prof. G. De Micheli
Academic Year: 07/08, 06/07
 - Course: Validation and Verification - Graduate course (taught in English)
Teacher: prof. F. Somenzi
Academic Year: 06/07, 05/06, 04/05
- University: Universtia' degli Studi di Milano (Crema, Italy)
 - Course: Sistemi Operativi (Operating System) - Undergraduate Course
Teacher: prof. V. Piuri
Academic Year: 08/09, 07/08, 06/07, 05/06

3.3 Theses Supervision

- **Advisor of the following PhD Theses at Politecnico di Milano:**
 - *On the Role of Reconfigurable Systems in Domain-Specific Computing.*
Student: D. Conficconi. Politecnico di Milano, 17 Feb 2022;
 - *The Case for Reconfigurable Architectures in High-Performance Graph and Sparse Information Retrieval.*
Student: A. Parravicini. Politecnico di Milano, 17 Feb 2022;
 - *On the management of power and performance trade-offs in distributed cloud-native infrastructures.*
Student: R. Brondolin. Politecnico di Milano, 29 Oct. 2020;
 - *Hugenomic: Exploiting FPGAs as Hardware Accelerators in the Genomic Domain.*
Student: L. Di Tucci. Politecnico di Milano, 29 Oct. 2020;
 - *Optimising Data-Intensive Applications for Modern Hardware Platforms.*
Student: A. Scolari. Politecnico di Milano, 6 Feb 2019;
 - *On How to Design Optimized Spatial Architectures: from Iterative Stencils to Convolutional Neural Networks.*
Student: G. Natale. Politecnico di Milano, 6 Feb 2019;
 - *CAOS: CAD as an Adaptive Open-platform Service for High Performance Reconfigurable Systems.*
Student: M. Rabozzi. Politecnico di Milano, 6 Feb 2019;
 - *On How to Effectively Target FPGAs from Domain Specific Tools.*
Student: E. Del Sozzo. Politecnico di Milano, 6 Feb 2019;
 - *Enabling power-awareness for multi-tenant systems.*
Student: M. Ferroni. Politecnico di Milano, 22 Feb 2017;
 - *On the design of autonomic techniques for runtime resource management in heterogeneous systems.*
Student: G. C. Durelli. Politecnico di Milano, 5 Feb 2016;
 - *On the role of polyhedral analysis in high performance reconfigurable hardware based computing systems.*
Student: R. Cattaneo. Politecnico di Milano, 17 Dec 2015;
 - *Techniques and Tools for Efficient, Qos-Driven Warehouse-Scale Computing.*
Student: D. B. Bartolini. Politecnico di Milano, 16 Feb 2015;
 - *System Support for Adaptive Performance and Thermal Management of Chip-Multiprocessors.*
Student: F. Sironi. Politecnico di Milano, 21 March 2014;
- **Advisor of the following PhD Students, still enrolled in the program at Politecnico di Milano: 8 (+3 starting in Nov, 2022)**
- **Advisor of the following Master Theses in CS at UIC, from 2008: 35**
- **Advisor of Master Theses in Computer Engineering at Politecnico di Milano, from 2009: 71**
- **Advisor of Master Theses in Biomedical Engineering at Politecnico di Milano, from 2016: 10**
- **Advisor of Master Theses in Electrical Engineering at Politecnico di Milano, from 2018: 2**
- **Advisor of Bachelor Theses in Biomedical Engineering at Politecnico di Milano, from 2013: 74**
- **Advisor of Bachelor Theses in CS at Politecnico di Milano, during the years 2008 - 2014: 33**
- **Co-Advisor of the following Master Theses:**
From 2005 until today, Marco D. Santambrogio has been the co-advisor of more than 20 CS students for their M.Sc. thesis works at Politecnico di Milano

- **Co-Advisor of the following Bachelor Theses:**

From 2005 until today, Marco D. Santambrogio has been the co-advisor of more than 80 CS students for their bachelor thesis works at Politecnico di Milano

4 SCIENTIFIC RESPONSIBILITY FOR FUNDED RESEARCH PROJECTS AND AWARDS

4.1 Research Grants:

- **Huawei Technologies Switzerland AG**
Project Title: Templated Spatial Architectures.
Period: Sept 2021 - Dic 2022
Funding: 204K \$
Santambrogio's role in the project: Principal Investigator
- **Oracle Labs**
Project Title: Leveraging accelerators for efficient data processing in the cloud through GrCUDA enhancements and maintenance.
Period: Jun 2021 - June 2022
Funding: 150K \$
Santambrogio's role in the project: Principal Investigator
- **Oracle Labs**
Project Title: Leveraging accelerators for efficient data processing in the cloud.
Period: Feb 2020 - Feb 2021
Funding: 100K \$
Santambrogio's role in the project: Principal Investigator
- **Oracle Labs**
Project Title: Enabling real-time accurate entity linking and other analytics on knowledge graphs.
Period: June 2018 - June 2020
Funding: 200K EUR (100K EUR per year)
Santambrogio's role in the project: Principal Investigator
- **H2020 EXTRA European project.**
PoliMi PI: M. D. Santambrogio
Period: Sept 2015 - Sept 2018
Funding: 450K EUR
Santambrogio's role in EXTRA:
 - PoliMi PI for EXTRA
 - General Assembly Member of the EXTRA project
 - Work package Leader of WP4 (*Development of Reconfigurable Tools Platform*)
- **FP7 SAVE European project.**
PoliMi PI: Prof. C. Bolchini (cristiana.bolchini@polimi.it)
Period: Sept 2013 - Sept 2016
Santambrogio's role in SAVE:
 - Task Leader of the following tasks: T3.1 (*Adaptive host OS components*) and T3.2 (*Adaptation policies/strategies*)
- **FP7 FASTER European project.**
PoliMi PI: Prof. D. Sciuto (donatella.sciuto@polimi.it)
Period: Sept 2011 - Dec 2014
Santambrogio's role in EXTRA:
 - Work package Leader of WP2 (*High-level analysis and reconfigurable system definition*)
 - Task Leader of the following tasks: T2.2 (*Application task profiling and identification of reconfigurable cores*) and T2.4 (*Compile-time baseline scheduling and core mapping onto reconfigurable regions*)
- **Fondazione Cariplo - Regione Lombardia**
Project Title: A Challenges Driven Design for Effective and Efficient Autonomic Mobile Computing Architectures.

Period: Oct 2016 - March 2018
Funding: 100K EUR
Santambrogio's role in the project: Principal Investigator

- **Humanitas**

Project Title: HUNA: Humanitas University NECST Application
Period: Dec 2016 - Jun 2018
Funding: 75K EUR
Santambrogio's role in the project: Principal Investigator

- **MathWorks Academic Support**

Project Title: Teaching computer programming and embedded systems with audio processing in MATLAB.
Period: Sept 2016 - Jun 2017
Funding: 38K EUR
Santambrogio's role in the project: Principal Investigator

- **Progetto Rocca Workshops and Colloquia.**

Collaboration between the MIT-CARBON Group and Politecnico di Milano - DRESO Group.
Period: January 2010
Funding: 25K USD

- **Swiss NSF Research Project (Division II).**

Project title: *Dynamically Adaptive Architectures for Nomadic Embedded Systems*.
Period: 02/2010 - 01/2013.
Partners: EPFL, Prof. David Atienza, in cooperation with Politecnico di Milano (IT): Prof. Donatella Sciuto and Dr. Marco D. Santambrogio.

- **HiPEAC Collaboration Grant.**

Title of the research: Self-Aware Reconfigurable Computing Systems for Energy Saving and Performance Enhancement.
Period: November 2010 - December 2011
Funding: 5K EUR

- **HiPEAC Collaboration Grant.**

Title of the research: Self-aware and autonomic system.
Period: July 2009
Funding: 5K EUR

4.2 Awards

- Advisor of the PhD category winners of the **Xilinx Open Hardware Contest 2020**. (PhD Category winner "*Personalized PageRank low-latency Recommender Systems*", [<http://www.openhw.eu/2020-results.html>])
- Co-author of the paper winner of the **BHI 2019 Best Paper Award**. ("*circFA: a FPGA-based circular RNA aligner*". [<https://ieeexplore.ieee.org/document/8834539>])
- Advisor of the AWS EC2 F1 category winners of the **Xilinx Open Hardware Contest 2018**. (AWS EC2 F1 Category winner "*5 Points to Rule Them All*", [<http://www.openhw.eu/2018-finalists.html>])
- Advisor of the PhD category winners of the **Xilinx Open Hardware Contest 2017**. (PhD Category winner "*bibbidi N-BObbiDY boo: Magic Acceleration of N-Body Simulation*", [www.openhw.eu/2017-finalists.html])
- Advisor of the PhD and Student FPGA category winners of the **Xilinx Open Hardware Contest 2016**. (PhD Category winner "*exaFPGA: Iterative stencil cell loop acceleration*", Student FPGA Category winner *ProFAX: Protein folding on FPGA* [www.openhw.eu/2016-finalists.html])
- Co-author of the paper winner of the **RAW 2016 Best Demo Award**. ("*On the Automation of High Level Synthesis of Convolutional Neural Networks*". [[30]])

- Co-author of the paper winner of the **EWiLi 2013 Best Paper Award**. (*"A Performance-Aware Quality of Service-Driven Scheduler for Multicore Processors"*. [[25]])
- Co-author of the paper winner of the **2012 HiPEAC Paper Award**. (*"Metronome: Operating System Level Performance Management via Self-Adaptive Computing"*. [[122]])
- Co-author of the **Best Student Paper award sponsored by IEEE TCPP**: 7th IEEE International Conference on Autonomic Computing (ICAC) 2010 (*Smartlocks: Lock Acquisition Scheduling for Self-Aware Synchronization* [[130]])
- Co-author of the Best Paper Award Finalist, IEEE International Conference on Field Programmable Logic and Applications (FPL) 2009 (*A Runtime Relocation Based Workflow for Self Dynamic Reconfigurable Systems Design* [[146]])
- December, 2008. awarded a **Progetto Rocca Postdoc Fellowship at MIT**.
- **Dimitri N. Chorafas PhD Thesis Award** from the Chorafas Foundation (Berne, Switzerland) for the best PhD Theses in "Systems Engineering and Information Technology", May 2008. Thesis title: *Hardware/Software codesign methodologies for dynamically reconfigurable systems*)
- Co author of the **Best paper award**: 15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007 (*ReCPU: a Parallel and Pipelined Architecture for Regular Expression Matching* [[170]])

5 TECHNOLOGY TRANSFER

5.1 Startups and Spin-Offs

- **Huxelerate**
Company name: Huxelerate S.R.L.
Company website: <https://www.huxelerate.it/>
Founded: Feb 2, 2019
Revenue in 2020: 0K EUR
Santambrogio's role in Huxelerate: Co-Founder & Scientific Advisor
Co-Founders: Lorenzo Di Tucci, Sara Notargiacomo, Marco Rabozzi, Marco Santambrogio
- **Arox**
Company name: Arox S.R.L.
Company website: <https://arox.io/>
Founded: November 28, 2018
Revenue in 2020: 300K EUR(60K EUR income)
Santambrogio's role in Huxelerate: Co-Founder & Scientific Advisor
Co-Founders: Niccoló Consolazio, Sara Notargiacomo, Luca Paccani, Marco Santambrogio, Davide Toschi

5.2 Patents

- **ID: US-2019102233-A1**
Title: Method for power optimization in virtualized environments and system implementing the same
Assignee: Politecnico Di Milano
Inventor/Author: MARCO D. SANTAMBROGIO, Matteo Ferroni, Marco Arnaboldi
Priority date: 2017-10-04
Filing/creation date: 2017-10-04
Publication date: 2019-04-04
Result link: <https://patents.google.com/patent/US20190102233A1/en>
- **ID: WO-2020217200-A1**
Title: Method of aligning strings of characters representing genomic data and related hardware device
Assignee: Huxelerate S.R.L.
Inventor/Author: Alberto Zeni, Matteo Crespi, Lorenzo Di Tucci, MARCO D. SANTAMBROGIO, Fabio Pizzato
Priority date: 2019-04-23
Filing/creation date: 2020-04-23
Publication date: 2020-10-29
Result link: <https://patents.google.com/patent/WO2020217200A1/en>
- **ID: WO-2019116213-A1**
Title: Method for locating a device inside an area
Assignee: Politecnico Di Milano
Inventor/Author: Donatella Sciuto, MARCO D. SANTAMBROGIO, Alessandro Antonio Nacci, Alessandro Frossi, Niccoló Consolazio, Luca Paccani, Andrea Cirigliano
Priority date: 2017-12-11
Filing/creation date: 2018-12-11
Publication date: 2019-06-20
Result link: <https://patents.google.com/patent/WO2019116213A1/en>
- **ID: WO-2020234792-A1**
Title: Système fpga-as-a-service pour informatique sans serveur accéléré
Assignee: Politecnico Di Milano
Inventor/Author: MARCO D. SANTAMBROGIO, Rolando Brondolin, Marco Bacis
Priority date: 2019-05-21
Filing/creation date: 2020-05-20
Publication date: 2020-11-26
Result link: <https://patents.google.com/patent/WO2020234792A1/fr>

- **ID: WO-2020217201-A1**

Title: Procédé de réalisation d'un dispositif matériel pour exécuter des opérations définies par un code logiciel de haut niveau

Assignee: Huxelerate S.R.L.

Inventor/Author: Marco Siracusa, Marco Rabozzi, Lorenzo Di Tucci, MARCO D. SANTAMBROGIO, Fabio Pizzato

Priority date: 2019-04-26

Filing/creation date: 2020-04-23

Publication date: 2020-10-29

Result link: <https://patents.google.com/patent/WO2020217201A1/fr>

6 PUBLICATIONS

6.1 Productivity and Impact Metrics

- Scientific Productivity: 300+ publications (303 entries on Scopus, 448 co-authors according to Scopus):
- Author/Co-author of 13 top-ranked Q1 journal papers (including IEEE Transactions on Control Systems Technology, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE Micro, ACM Transactions on Autonomous and Adaptive Systems, ACM Transactions on Embedded Computing Systems (TECS), IEEE Transactions on Emerging Topics in Computing, ACM Computing Surveys (CSUR), and IEEE Transaction. on CAD of Integrated Circuits and Systems) from SCIMAGO ([HTTP://SCIMAGOJR.COM](http://scimagojr.com))
- Author/Co-author of 250+ scientific publications on peer-reviewed conferences including 57 top-level A1/A2 Class 1 conferences (ASP-DAC, CODESS+ISSS, DAC, DATE, FCCM, FPGA, FPL, ICAC, ICCAD, IPDPS, ISCAS, OSDI, PACT, PPOPP, UbiComp) from Conference Ranks ([HTTP://WWW.CONFERENCERANKS.COM/#DATA](http://www.conferencerranks.com/#data)).
- Publication Impact:
 - Based on Google Scholar: h-index 37, citations 4981
 - Based on Scopus: h-index 25, citations 2616

6.2 List of all the publications

Book

- [1] Pao-Ann Hsiung, M. D. SANTAMBROGIO, and Chun-Hsian Huang. *Reconfigurable System Design and Verification*. Taylor & Francis/CRC Press, 2009.

Journals

- [1] Davide Conficconi, Emanuele Del Sozzo, Filippo Carloni, Alessandro Comodi, Alberto Scolari, and Marco Domenico Santambrogio. “An energy-efficient domain-specific architecture for regular expressions”. In: *IEEE Transactions on Emerging Topics in Computing* (2022).
- [2] Eleonora D’Arnese, Guido Walter Di Donato, Emanuele Del Sozzo, Martina Sollini, Donatella Sciuto, and Marco Domenico Santambrogio. “On the automation of radiomics-based identification and characterization of nsclc”. In: *IEEE Journal of Biomedical and Health Informatics* 26.6 (2022), pp. 2670–2679.
- [3] Daniele Parravicini, Davide Conficconi, Emanuele Del Sozzo, Christian Pilato, and Marco D Santambrogio. “CICERO: A Domain-Specific Architecture for Efficient Regular Expression Matching”. In: *ACM Transactions on Embedded Computing Systems (TECS)* 20.5s (2021), pp. 1–24.
- [4] Enrico Reggiani, Emanuele Del Sozzo, Davide Conficconi, Giuseppe Natale, Carlo Moroni, and Marco D Santambrogio. “Enhancing the scalability of multi-fpga stencil computations via highly optimized hdl components”. In: *ACM Transactions on Reconfigurable Technology and Systems (TRETs)* 14.3 (2021), pp. 1–33.
- [5] Marco Siracusa, Emanuele Delsozzo, Marco Rabozzi, Lorenzo Di Tucci, Samuel Williams, Donatella Sciuto, and Marco Domenico Santambrogio. “A Comprehensive Methodology to Optimize FPGA Designs via the Roofline Model”. In: *IEEE Transactions on Computers* (2021).
- [6] Samuele Barbieri, Fabiola Casasopra, Rolando Brondolin, and MARCO DOMENICO SANTAMBROGIO. “FARD: accelerating distributed fog computing workloads through embedded FPGAs”. In: *ACM SIGBED Review* 17.1 (2020), pp. 56–62.

- [7] Rolando Brondolin, Marco Arnaboldi, and MARCO DOMENICO SANTAMBROGIO. “Power consumption management under a low-level performance constraint in the Xen hypervisor”. In: *ACM SIGBED Review* 17.1 (2020), pp. 42–48.
- [8] Rolando Brondolin and MARCO DOMENICO SANTAMBROGIO. “A Black-box Monitoring Approach to Measure Microservices Runtime Performance”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 17.4 (2020), pp. 1–26.
- [9] Luca Cerina and MARCO DOMENICO SANTAMBROGIO. “SAGE: a configurable code generator for efficient symbolic analysis of time-series”. In: *ACM SIGBED Review* 17.1 (2020), pp. 12–17.
- [10] Luca Cerina, MARCO DOMENICO SANTAMBROGIO, Giuseppe Franco, Claudio Gallicchio, and Alessio Micheli. “EchoBay: Design and optimization of echo state networks under memory and time constraints”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 17.3 (2020), pp. 1–24.
- [11] Luca Stornaiuolo, Filippo Carloni, Riccardo Pressiani, Giuseppe Natale, MARCO DOMENICO SANTAMBROGIO, and Donatella Sciuto. “Enabling transparent hardware acceleration on Zynq SoC for scientific computing”. In: *ACM SIGBED Review* 17.1 (2020), pp. 30–35.
- [12] F Barbic, M Minonzio, B Cairo, D Shiffer, A Dipasquale, L Cerina, A Vatteroni, V Urechie, P Verzeletti, F Badilini, et al. “Effects of different classroom temperatures on cardiac autonomic control and cognitive performances in undergraduate students”. In: *Physiological measurement* 40.5 (2019), p. 054005.
- [13] Rolando Brondolin, Matteo Ferroni, and MARCO DOMENICO SANTAMBROGIO. “Performance-aware load shedding for monitoring events in container based environments”. In: *ACM SIGBED Review* 16.3 (2019), pp. 27–32.
- [14] Cristiana Bolchini, Stefano Cherubin, Gianluca C Durelli, Simone Libutti, Antonio Miele, and MARCO DOMENICO SANTAMBROGIO. “A runtime controller for OpenCL applications on heterogeneous system architectures”. In: *ACM SIGBED Review* 15.1 (2018), pp. 29–35.
- [15] Matteo Ferroni, Juan A Colmenares, Steven Hofmeyr, John D Kubiawicz, and MARCO DOMENICO SANTAMBROGIO. “Enabling power-awareness for the xen hypervisor”. In: *ACM SIGBED Review* 15.1 (2018), pp. 36–42.
- [16] Matteo Ferroni, Andrea Corna, Andrea Damiani, Rolando Brondolin, John D Kubiawicz, Donatella Sciuto, and Marco D Santambrogio. “MARC: a resource consumption modeling service for self-aware autonomous agents”. In: *ACM Transactions on Autonomous and Adaptive Systems (TAAS)* 12.4 (2017), pp. 1–29.
- [17] M. Rabozzi, G. C. Durelli, A. Miele, J. Lillis, and MARCO DOMENICO. SANTAMBROGIO. “Floorplanning Automation for Partial-Reconfigurable FPGAs via Feasible Place-ments Generation”. In: *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)* 25.1 (2017), pp. 151–164. ISSN: 1063-8210. DOI: 10.1109/TVLSI.2016.2562361.
- [18] Riccardo Cattaneo, Giuseppe Natale, Carlo Sicignano, Donatella Sciuto, and MARCO DOMENICO. SANTAMBROGIO. “On How to Accelerate Iterative Stencil Loops: A Scalable Streaming-Based Approach”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 12.4 (2016), p. 53. DOI: 10.1145/2842615. URL: <http://doi.acm.org/10.1145/2842615>.
- [19] Gianluca C. Durelli and MARCO DOMENICO. SANTAMBROGIO. “Autonomic thread scaling library for QoS management”. In: *SIGBED Review* 13.1 (2016), pp. 41–47. DOI: 10.1145/2907972.2907978. URL: <http://doi.acm.org/10.1145/2907972.2907978>.
- [20] Alberto Scolari, Davide Basilio Bartolini, and MARCO DOMENICO. SANTAMBROGIO. “A Software Cache Partitioning System for Hash-Based Caches”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 13.4 (Dec. 2016), 57:1–57:24. ISSN: 1544-3566. DOI: 10.1145/3018113. URL: <http://doi.acm.org/10.1145/3018113>.

- [21] Dionisios N. Pnevmatikatos, Kyprianos Papadimitriou, Tobias Becker, Peter Böhm, Andreas Brokalakis, Karel Bruneel, C. Ciobanu, Tom Davidson, Georgi Gaydadjiev, Karel Heyse, Wayne Luk, Xinyu Niu, Ioannis Papaefstathiou, Danilo Pau, Oliver Pell, Christian Pilato, MARCO DOMENICO. SANTAMBROGIO, Donatella Sciuto, Dirk Stroobandt, Tod Todman, and Elias Vansteenkiste. “FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration”. In: *Microprocessors and Microsystems - Embedded Hardware Design* 39.4-5 (2015), pp. 321–338. DOI: 10.1016/j.micpro.2014.09.006. URL: <http://dx.doi.org/10.1016/j.micpro.2014.09.006>.
- [22] Davide B. Bartolini, Filippo Sironi, Donatella Sciuto, and MARCO DOMENICO. SANTAMBROGIO. “Automated Fine-Grained CPU Provisioning for Virtual Machines”. In: *ACM Transactions on Architecture and Code Optimization (TACO)* 11.3 (2014), 27:1–27:25. DOI: 10.1145/2637480. URL: <http://doi.acm.org/10.1145/2637480>.
- [23] Xabier Iturbe, Ali Ebrahim, Khaled Benkrid, Chuan Hong, Tughrul Arslan, Jon Perez, Didier Keymeulen, and MARCO DOMENICO. SANTAMBROGIO. “R3TOS-Based Autonomous Fault-Tolerant Systems”. In: *IEEE Micro* 34.6 (2014), pp. 20–30. DOI: 10.1109/MM.2014.58. URL: <http://dx.doi.org/10.1109/MM.2014.58>.
- [24] Jacopo Panerati, Martina Maggio, Matteo Carminati, Filippo Sironi, Marco Triverio, and MARCO DOMENICO. SANTAMBROGIO. “Coordination of Independent Loops in Self-Adaptive Systems”. In: *ACM Transaction on Reconfigurable Technology and Systems (TRETs)* 7.2 (2014), 12:1–12:16. DOI: 10.1145/2611563. URL: <http://doi.acm.org/10.1145/2611563>.
- [25] Filippo Sironi, Donatella Sciuto, and MARCO DOMENICO. SANTAMBROGIO. “A performance-aware quality of service-driven scheduler for multicore processors”. In: *SIGBED Review* 11.1 (2014), pp. 50–55. DOI: 10.1145/2597457.2597464. URL: <http://doi.acm.org/10.1145/2597457.2597464>.
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