Andrea Giovanni Bonfanti

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EDUCATION

- In 1991, "Diploma" degree at Liceo Scientifico, M. G. Agnesi in Merate (LC)
- In 1999, "Laurea Degree" (5-Year degree) in Electronic Engineering, *summa cum laude* (100/100) with a dissertation on "*Frequency instability in fully-integrated oscillators for wireless application*" at the Politecnico di Milano, Milan, Italy
- In 2003, “Ph.D. degree” in Electronics and Communications from the Politecnico di Milano with a dissertation on "*Conversion mechanisms of low frequency noise into phase noise in fully-integrated LC tuned oscillator*"

CURRENT POSITION

At the present time he is Associate Professor at Dipartimento di Elettronica, Informazione e Bioingegneria of the Politecnico di Milano, where he is involved in a three-fold activity:

1) design of low-power and low-voltage analog/mixed integrated circuits for acquisition, filtering and digital conversion of neural signal;
2) design of integrated circuits for sensing and driving MEMS-based magnetometers and gyroscope:
3) sudy and design of low phase noise oscillators with particular enphasis on flicker-induced phase noise minimization.

EXPERIENCES IN ACADEMIC AND RESEARCH INSTITUTES

- From 2003 to 2006 he was Post-Doctoral Researcher at the Dipartimento di Elettronica e Informazione of the Politecnico di Milano involved in the design of fully-integrated RF circuits (oscillators and frequency synthesizers for wireless applications).

- From 2007 to 2008 he was Post-Doctoral Researcher at the Dipartimento di Elettronica e Informazione of the Politecnico di Milano designing analog front-end circuits (amplifiers and AD converters) for recording neural signals from human brain.

- From 2008 to 2009 he was Senior Post-Doctoral researcher at the Italian Institute of Technology (IIT, Genova), involved in the design of integrated circuits and electronic systems for acquisition and elaboration of neural signals both in small animals and human patients.

- From 2009 to 2011 he was Temporary Assistant Professor at the Dipartimento di Elettronica e Informazione of the Politecnico di Milano.

- From 2011 to 2015 he was Associate Professor at the Dipartimento di Elettronica e Informazione of the Politecnico di Milano.

INDUSTRIAL EXPERIENCES

- In 2003 he worked as a consultant for the RF group of ST-Microelectronics, Catania, Italy, on the realization of a 3GHz Clapp-VCO followed by a bipolar frequency doubler
- In 2006 he worked as a consultant for CEFRIEL (Center of Excellence for Research, Innovation, Education and industrial Labs partnership), Milano, Italy, on the realization of DC-DC converters and microstrip integrated sensors for PC and cellular

PROFESSIONAL SKILLS

- Analysis and design of schematic and layout of analog/RF ICs in both CMOS and BiCMOS technology with CAD tools (Cadence, Spectre, Eldo, Spice, Virtuoso, Calibre, Diva, Verilog).
- Design of digital integrated circuits with semi-automated design tool based on VHDL code and place-and-route of standard cells.
- System development and analysis through high-level behavioral simulations (Simulink, Matlab, VerilogA). Definition of block specifications from architectural analysis.
- Design of analog, mixed-signal and RF multilayer test boards for test chip measurements.
- Development of experimental set-up for analog, mixed-signal and RF measurements.

INTEGRATED CIRCUIT IMPLEMENTATION

- 2 Phase Locked Loop (PLL) frequency synthesizers
- 28 voltage controlled oscillators in the 900MHz-15GHz frequency range
- 1 Analog Sigma-Delta modulator for DECT receiver
- 15-GHz quadrature injection locked divider
- 5-GHz frequency doubler
- 1 Switched-Capacitor front-end for neural signal acquisition
- 16-channel low-noise low-power amplifier array and AD converter for neural signal acquisition
- 1 all-analog integrated circuit for amplification, detection and extraction of neural spike features
- 1 integrated circuits for amplification, digitization, compression and wireless transmission of neural spikes
- 1 integrated circuits for amplification, digitization and UWB wireless transmission of LFPs and neural spikes
- 2 low-power low-voltage SAR AD converters
- 1 low-power analog front-end for Lorentz force based magnetometer
- 1 low-power analog front-end and AD converter for a three axis magnetometer based on an anisotropic magneto-resistive sensor (AMR)
- 1 MEMS-based oscillator
- 2 integrated circuits for acquisition of local-field-potentials (LFPs) to treat Parkinson’s disease

PATENTS

1 national patent “Neurostimolatore elettrico” (A. Spinelli, A. Bonfanti, R. Gusmeroli, T. Borghi and L. Fadiga)

EDITORIAL ACTIVITY

He acts as reviewer for the following journals:

- IEEE Transaction on Circuits and Systems I – Regular Papers
- IEEE Transaction on Circuits and Systems II – Express Briefs
- IEEE Transaction on Microwave Theory and Techniques
- IEEE Journal of Solid State Circuits
- ELSEVIER Microelectronic Journal

RESEARCH ACTIVITY

2013-now *Design of low-power analog front-ends and AD converters for sensing and driving MEMS-based magnetometers and gyroscopes.*

Magnetomters and gyroscopes are essential sensors in comsumer electronics and are widely adopted to implement digital compasses or 9-axis inertial measurement units (IMUs).

Magnetometers are typically developed exploiting anisotropic magneto-resistance (AMR) technologies or Hall-effect. In the framework of ENIAC - 325622 “LAB FAB for smart sensors and actuators MEMS” project, a new solution, i.e. Lorentz force based MEMS magnetometer, has been investigated in collaboration with ST-Microelectronics and the “SandLab” research group at the Dipartimento di Elettronica, Informazione e Bioingegnera at the Politecnico di Milano. This approach is encouraged by the possibility to integrate magnetic sensors in the same MEMS technology already used for gyroscopes and accelerometers, so to design a complete 9-axis IMU in a single process, avoiding the use of magnetic materials and overcomimg noise densities reachable by Hall devices.

My activity was focused on the design of the read-out and driving electronics of the Lorentz force-based magnetometer. Due to an intrinsic lower noise with respect to other magnetic sensors but also a lower sensitivity, an extremely loiw-noise and low-power read-out eletronics is mandatory to detect the weak signal (typically a capacitance variation in the order of aF) without degrading the signal-to-noise ratio. The problem related to a reduced sensitivity is exhacerbated driving the sensor out of resonance to break the trade-off between sensing bandwidth and noise. To this aim, I develop a very low-noise low-power analog front-end to be coupled in a system-in-package with the MEMS device in order to sense and drive the magnetometer [20, 52]. This is the first system (magnetometer plus read-out/drive electronics) presented in literature and with performance suited for consumer applications.

On the other hand, frequency-modulated (FM) gyroscopes have been realized as angular rate sensors based on Coriolis force, where the rate information is frequency-modulated onto the resonance frequency of the MEMS structure. FM operation promises ultra-stable ratiometric sensitivity and reduced calibration costs. This would provide benefits in applications, e.g. inertial navigation, where stability is of great concern. In this framework

we have implemented a fully integrated low-power oscillator for FM operation, and its coupling to an axisymmetric, push-pull, differential-sense Z-axis gyroscope fabricated in a standard process commonly used for mass production of inertial sensors [55].

2015-2016 *Study and design of Successive-Approximation Register Charge Redistribution (SAR-CR) analog to digital converters*

The implementation of a high resolution (>10 bit) analog-to-digital converter (ADC) with a successive approximation register charge redistribution (SAR-CR) topology has been investigated. SAR-CR converters are widely adopted for medium resolution (8-10 bit) and medium speed(<10Mbps) applications. Larger resolutions are typically accomplished with ΣΔ converters, which are more power demanding and less prone to benefit to technology scaling than SAR-CR architectures [54]. On the other hand, the latters are typically limited by the linearity of the feedback digital-to-analog converter tybased on a charge-redistribution capacitive array and by the effect of the parasitic capacitances. To this aim, a Matlab-based tool has been developed to perform both parametric and statistical simulations taking into account capacitive mismatch and parasitic capacitances in order to compute both differential- (DNL) and integral nonlinearity (INL), SNDR and number of effective bits [23,49,50,53]. This tool allows to overcome the traditional heavy and impractical simulations performed in common circuit design environments.

In this framework, two SAR ADCs have been implemented and succesfully tested.

A 10-bit asynchronous fully-differential SAR ADC with attenuation capacitor been fabricated in a standard 0.13-nm CMOS technology. At a 0.5-V supply and 200-kSps sampling frequency, the ADC achieves a SNDR of 52.6 dB, an ENOB of 8.45, and a power consumption of 420 nW, corresponding to a figure-of-merit (FOM) of 6 fJ/conversion-step [18,51]. This efficiency is comparable to the best results published so far and it's the lowest among ADCs in 130-nm or less scaled technology.

A second SAR ADC has been integrated in a 0.35-μm CMOS process to prove the feasibility of such converters featuring a SNDR larger than [22]. The proposed ADC exploits a semi-custom and isotropic unit capacitance with ground shield to avoid proximity effects and parasitic capacitances across its terminals, an optimized capacitive array layout insensitive to both linear and radial oxide gradients, and an efficient calibration algorithm to compensate the parasitic capacitances that worsen the converter linearity. At 1.8-V supply and 100-kSps sampling frequency, the proposed ADC achieves an SNDR of 70.7 dB, an SFDR of 81.8 dB, an ENoB of 11.45 and a power consumption of 43.4 μW, corresponding to a Figure-of-Merit (FoM) of 155 fJ/conv.step. This figure is the best among SAR converters implemented in 350-nm or less scaled technologies, and in-line with other ADCs featuring an SNDR larger than 70 dB.

2011-now *Analysis and minimization of flicker noise up-conversion of cyclostationary flicker noise in voltage-biased and current-biased multi-GHz oscillators*

The modulation of harmonic distortion due to the so-called Groskowski effect in voltage-biased oscillators (Van der Pol oscillators) has been identified as the primary cause of flicker noise up-conversion in voltage biased oscillator [11]. Two oscillator topologies have been integrated aiming to minimize flicker noise up-conversion without impairing the achievable tuning-range and worsening the white-induced phase noise [14,15,45,47]. Also, the up-conversion of 1/f noise in current-biased oscillator has been investigated. For this

class of oscillators the main mechanism of flicker up-conversion is due to the modulation of parasitic capacitances of the transconductor devices, which are amplitude-dependent capacitances, leading to a conversion of amplitude noise into frequency/phase noise Also the effect of the distributed flicker noise sources along the MOSFET transistor channel has been investigated [48].
In this framework, a fast and accurate simulation technique to evaluate the impulse sensitivity function (ISF) of oscillators has been developed. The proposed method, based on the linear-time variant (LTV) analysis of oscillators, computes the impulse phase response by means of periodic steady-state (PSS) and periodic transfer function (PXF) simulations available in commercial simulators (like Spectre, Eldo, etc.) [12,42,43]. This technique overwhelms the classical simulation method based on transient analysis and injection of charge pulses along the oscillator period in terms of both speed and precision. The method was then extended also to take into account the cyclostatinary nature of noise source in oscillators [44, 46].

2006-now *Study and realization of fully-implantable integrated circuits for acquisition, processing and wireless transmission of neural signal*

For extracellular recordings from neurons, a bandpass amplifier/filter is needed to amplify the detected signal. High gain, low noise and selective filtering in the band of interest (100Hz-10kHz) with a very low power budget are required to properly read out the weak neural signals (about 10μV-1mV) in a noisy environment. In this framework, an integrated version of a low noise band-pass amplifier employing subthreshold MOS transistors as pseudo-resistor elements to implement a very low cut-off frequency has been integrated and tested showing the best trade-off between power consumption and noise [37].
Moreover, since a brain machine interface requires a multichannel system for recording from a large number of neurons and neural spikes are rare events (10-100 spikes per second with time length of about 1msec), an analog circuit able to detect neural activity and extract from each neural spike the main features, i.e. amplitude and time width, has been implemented [38,39]. The detection is based on a novel spike detection algorithm while the feature extraction is performed by a high precision peak-detector and a time to amplitude converter. The developed circuits were firstly tested in in-vitro experiments with cultures of neurons at the Dipartimento di Chimica at the Politecnico di Milano and then in in-vivo experiments at the Dipartimento di Fisiologia at the Università degli Studi di Ferrara (with Prof. Luciano Fadiga) and at the Italian Institute of Technology (Genova). He collaboration with IIT in the framework of the Brain Machine Interface project brought to the development of a multi-channel system-on-chip (SoC) able to acquire signal from many electrodes implanted in the somatosensory cortex of small laboratory animals [35,36] and to send in wired mode the data to a remote host in order to parse the acquired data.
The next step was to develop a SoC able to wirelessly transmit the signals acquired from a large population of neurons. In fact, wireless multi-channel neural recording systems are highly needed in both neuroscience experiments and in prosthetic applications. In neuroscience, their adoption improves animal freedom of movements and reduces motion artifacts and tethering effects. In neuroprosthetics, wireless solutions are more immune to infection. To this aim, the activity was focused on digital processing of the amplified/filtered neural signals. This operation is mandatory in order to reduce the huge amount of data, especially for system with more than 100 channels, and to enable a low-power wireless data transmission [9]. Compression of the raw data is implemented by

detecting the action potential (AP) spikes and storing up to 20 points for each waveform. Thanks to this digital data compression algorithm, a multi-channel neural spike recording system-on-chip with wireless telemetry has been integrated and successfully tested [13,40, 41]. The system includes 64 low-noise analog amplifiers, a time-division multiplexer, a single 8-bit SAR ADC, followed by the digital signal compression and a transmission unit. The latter exploits a 400-MHz VCO and adopts a Manchester-Coded Frequency Shift Keying (MC-FSK) with low modulation index. In this way a 1.25-Mbit/s data rate is delivered within a band of about 3-MHz. This integrated circuit has been adopted at the Italian Institute of Technology (IIT) to perform experiments on rats and mice to study the complex behavior of the brain [10] and to implement a closed-loop system able to sense the neural signal and delver pulses of current to stimulate the animals while accomplishing different tasks, like grasping the food [17]. The same integrated circuit has been adopted also in surgery rooms with human patients affected by brain tumor to detect neural activity [19].

This first wireless prototype has been the ancestor of a second SoC, implemented in a more scaled technology (0.13μm CMOS from UMC) with superior performance in terms of power consumption and amount of data transmitted. This new system is able to acquire neural signals from 64 channels and transmit a data stream of 20Mbps (20kHz per channel with a 10-bit resolution) without performing data compression and thus degrading the quality of the acquired signal. This has been made possible by implementing a UWB transmitter in collaboration with the Università di Padova (Prof. Andrea Neviani and Prof. Andrea Bevilacqua). This SoC features the lowest power per channel and the largest transmission range among state-of-the-art wireless neural recording systems [21].

2002-2006 *Study and realization of a PLL+DDS architecture for third generation wireless systems.*

The possibility to implement a frequency synthesizer that meets the third generation wireless systems requirements (fast channel settling, low phase noise and spurs) with a PLL+DDS architecture has been studied. The low frequency synthesized by a DDS (Direct Digital Synthesis) is locked and translated at high frequency by a wideband and integer divider PLL. Before integration, this new architecture has been realized assembling monolithic circuits (divider, VCO, DDS, PFD) in a test board [3]. An integrated version of the whole PLL synthesizer together with the DDS and the digital-to-analog converter has been designed and realized in BiCMOS 0.35μm technology and successfully tested [8].

2005-2003 *Design of a multistandard PLL for 802.11a-b-g and HIPERLAN2 WLAN applications*

The emerging cellular and wireless standards need the development of multi-mode transceiver systems. The main challenge in such systems is to own a common frequency synthesizer to reduce the manufacturing cost and provide the target customers with a reasonable and cost-effective solution. The proposed and implemented frequency synthesizer [34] is a fractional-N PLL with a Sigma-Delta modulation to randomize fractional-N spurs. The voltage-controlled oscillator runs at 10-GHz and has a large tuning range (30%, from 8.7GHz to 12.3GHz) and low phase noise to fulfill the stringent requirements of WLAN standards based on OFDM. Digital-controlled varactors set the central oscillation frequency (coarse-tuning), whereas a small analog varactor is responsible of a fine tuning of the

oscillation frequency. The VCO is followed by two I-Q divider (x2) giving the 5-GHz and 2.5-GHz outputs. The dividers by 2 are realized as injection-locked ring oscillators [5,32]. A state-logic machine, named AFC (Automatic Frequency Control) controls the binary word of the VCO. The ΔΣ quantization noise folding is attenuated by using a linear charge-pump and a new compensation technique based on a delay introduced between the reference signal and the divider output.

2002 *Design of 3-GHz oscillator and frequency doubler for WLAN applications*

A bipolar VCO with phase noise high performance and wide tuning range followed by a frequency doubler for 802.11a WLAN standard has been designed for ST-Microelctronics in Si-Ge technology. The oscillator was designed with an external tank resonator avoiding the problem of multi-oscillation choosing a modified differential Clapp topology. The doubler was implemented connecting the collector of two common emitter bipolar transistors and using a resonant load tuned at the second harmonic of the oscillation [25].

2002 *Study of LC quadrature oscillators (QVCO) and in-phase coupled oscillators.*

The availability of accurate quadrature signals is a prerequisite for the implementation of image-rejection transceivers, which are mandatory to accomplish complete transceiver integration. The most popular method is to let the voltage-controlled oscillator (VCO), usually in the form of an LC-tank VCO, work at double the desired frequency, and then to obtain quadrature signals at the desired frequency via frequency division, performed either in the digital or in the analog domain. However, a more attractive approach in terms of power consumption and accuracy performance relies on the possibility of coupling two symmetric LC-tank VCOs to each other, thereby exploiting the good phase noise performance of LC-oscillators. The first and best known implementation of the quadrature VCO (QVCO) was proposed by Rofougaran et al. where coupling between two VCOs is enforced by transistors placed in parallel with the switch transistors [2]. In this framework, I proposed and studied in collaboration with Prof. Piero Andreani (Lund University) a new topology, named S-QVCO (series-QVCO) where coupling and transconductor transistors are placed in series. This topology allows better phase noise performance for the same error performance than traditional QVCOs. Furthermore, flicker noise up-conversion mechanisms in quadrature VCOs and the phase error accuracy due to tank element mismatch have been deeply analyzed and assessed [26].
Starting from the analysis of coupling between oscillators to get 90° phase shift between the output voltages, oscillators coupled in-phase were investigated in order to improve phase noise performance. In fact, forcing several LC oscillators to run in phase is a valuable means of achieving the wanted phase noise with practical values of inductances and capacitances. However, in-phase oscillator arrays suffer from the up-conversion of transistors' flicker noise in the presence of oscillator mismatches. Thus, a multitank oscillator topology was proposed [7,31], with superior tolerance to mismatches and avoiding any mechanism of flicker noise up-conversion (aside from the classical mechanism intrinsic in the nature of an oscillator).

2001-2002 *Study of flicker noise up-conversion in LC-tuned CMOS oscillators due to AM-to-PM conversion*

The up-conversion of flicker noise of the active elements in LC-tuned CMOS oscillators has been studied. Two different mechanisms are responsible to convert flicker noise coming from the bias current generator and from active elements in $1/f^3$ phase noise: AM-to-PM conversion and output common mode modulation. Both these effects mainly depend on the varactor characteristic and so this phenomenon assumes a great importance in low-power CMOS oscillators where the C-V characteristic is very steep [1].
In this framework, a new varactor topology, named back-to-back varactor configuration, has been proposed and integrated featuring a great reduction of AM-to-PM conversion mechanism without impairing the achievable tuning range [6, 29].
Another oscillator topology, employing a differential tuning, has been proposed to reduce the up-conversion of amplitude noise into phase noise caused by varactors non-linearity [4,30].

1999-2000 *Design of baseband Σ-Δ modulator for multistandard wireless receiver.*

The proposed *Σ-Δ* modulator converts the signal and the interferers reaching the receiver in a bit stream; the filtering and channel selection is demanded to the digital low pass filter (decimator) following the modulator. This filter may be implemented programmable to adapt at different wireless standard bandwidth requirements: the advantages over an analogue filter are obviously. The ADC converter has been implemented considering the tight requirements of DECT standard (channel bandwidth of 700kHz). It works at 33.6MHz to assure a minimum Over Sampling Ratio (OSR) of 24 and with a second order multibit structure. The designed modulator has a Signal-to-Noise plus Distortion (SNDR) and a Dynamic Range (DR) of 70dB, an IIP_3 of 18 BV and a power alimentation of 2V. This Σ-Δ implements a novel technique for dynamic element matching, named DIA (Double Index Averaging). The modulator has been integrated in an ALCATEL-MIETEC 0.35μm-CMOS technology.

1998-1999 *Study, characterization and optimization of phase noise in bipolar LC Voltage-Controlled Oscillators.*

The frequency instability and phase noise in bipolar LC-tuned VCO has been studied and experimentally verified on a 2.6-GHz fully integrated oscillator. The mechanisms involved in the generation of phase noise have been investigated: AM-to-PM conversion due to varactors, Groszkowski effect due to the non linearity of the active elements and "indirect instability" of the transconductor. A fast simulation technique for phase noise prediction has been proposed [27]. The need to quickly start the oscillation and to stabilize the amplitude of the waveform imposes the use of an AAC (Amplitude Automatic Control). The noise generated by the peak detector and by the amplifier of the AAC has been discussed and experimentally verified [28]. Also the relationship between phase noise and cycle-to-cycle jitter has been studied [24].

TEACHING ACTIVITIES

2001-2003 Teaching assistant of the 2nd course of Analog and Digital Electronics, "Elettronica II", (5-Year laurea degree, Prof. Andrea Lacaita) at the Politecnico of Milano.

2004 Teaching assistant of the course of "Microelettronica" (for the 3+2 year laurea degree, Prof. Mario Bertolaccini) at the Politecnico of Milano.

2004-2013 Teaching assistant of the course of "Progettazione Elettronica" (for the 3+2 year laurea degree, Prof. Andrea Lacaita) at the Politecnico of Milano. For this course he is author and co-author of four books [57-60].

2013-2015 Holder of the course ”Digital Integrated Circuit Design” (for the 3+2 year laurea degree) at the Politecnico of Milano.

THESIS AS ADVISOR OR CO-ADVISOR

PH.D. THESIS

- Federico Pepe, “Analysis and minimization of flicker noise up-conversion in LC tuned oscillators”, Ph.D. Dissertation, 2013, advisor Prof. Andrea Lacaita, co-advisor **Prof. Andrea Bonfanti**, Politecnico di Milano.
- Stefano Brenna, “Low-power, low-voltage, mixed-signal integrated circuits for smart sensors”, Ph.D. Dissertation, 2015, advisor Prof. Andrea L. Lacaita, co-advisor **Prof. Andrea Bonfanti**, Politecnico di Milano.

MASTER THESIS

- Massimo Maspero, “Studio dell’architettura di un modulatore ΣΔ multibit per applicazioni wireless e progetto del relativo integratore”, Master Thesis, 2000, advisor Prof. Andrea L. Lacaita, co-advisor **Dr. Andrea Bonfanti**, Politecnico di Milano.
- Flavia Amorosa, “Progetto e caratterizzazione di un nuovo sintetizzatore di frequenza DDS+PLL per applicazioni wireless”, Master Thesis, 2001, advisor Prof. Andrea L. Lacaita, co-advisor **Dr. Andrea Bonfanti**, Politecnico di Milano.
- Massimo Barni, “Sintetizzatore di frequenza multistandard a 12GHz per applicazioni wireless LAN”, Master Thesis, 2003, advisor Prof. Andrea L. Lacaita, co-advisor **Dr. Andrea Bonfanti**, Politecnico di Milano.
- Annamaria Tedesco, “Sintetizzatore di frequenza multistandard a 12GHz per applicazioni wireless LAN”, Master Thesis, 2004, advisor Prof. Andrea L. Lacaita, co-advisor **Dr. Andrea Bonfanti**, Politecnico di Milano.
- Alessandro Valerio, “Progetto e realizzazione di un sintetizzatore di frequenza multistandard per applicazioni WLAN”, Master Thesis, 2005, advisor Prof. Andrea L. Lacaita, co-advisor **Dr. Andrea Bonfanti**, Politecnico di Milano.
- Francesco Pini, “Analisi e progetti di circuiti integrati per l’amplificazione di segnali neuronali con sistema di alimentazione wireless”, Master Thesis, 2008, advisor Prof. Alessandro Sottocornola Spinelli, co-advisor **Dr. Andrea Bonfanti**, Politecnico di Milano.
- Tommaso D’amico, “Progetto e realizzazione di un convertitore analogico-digitale ad approssimazioni successive integrato per sistemi di acquisizione di segnali neuronali”, Master Thesis, 2008, advisor Prof. Alessandro Sottocornola Spinelli, co-advisor **Dr. Andrea Bonfanti**, Politecnico di Milano.

- Maria Ceravolo, “Progetto di un sistema integrato e impiantabile per il filtraggio, l’elaborazione e la compressione del segnale neuronale”, Master Thesis, 2008, advisor Prof. Alessandro Sottocornola Spinelli, co-advisor **Dr. Andrea Bonfanti**, Dott. Guido Zambra, Politecnico di Milano.
- Olga Settanni, “Progetto di un modulatore Sigma Delta per applicazioni ECG”, Master Thesis, 2008, advisor Prof. Alessandro Sottocornola Spinelli, co-advisor **Dr. Andrea Bonfanti**, Dott. Guido Zambra, Politecnico di Milano.
- Roberto Modaffari, “Meccanismi di conversione del rumore flicker in rumore di fase in oscillatori a filtro LC integrati”, Master Thesis, 2012, advisor Prof. Andrea Leonardo Lacaita, co-advisor **Prof. Andrea Bonfanti**, Politecnico di Milano.
- Stefano Brenna, “Front-end a basso consumo per l’acquisizione e la digitalizzazione di segnali neuronali”, Master Thesis, 2012, advisor Prof. Andrea L. Lacaita, co-advisor **Prof. Andrea Bonfanti**, Politecnico di Milano.
- Manuela Dellerba, “Progetto di un circuito integrato per la lettura e il pilotaggio di un magnetometro MEMS basato sulla forza di Lorentz e operante fuori risonanza” Master Thesis, 2014, advisor **Prof. Andrea Bonfanti**, co-advisor Dr. Stefano Brenna, Politecnico di Milano.
- Alireza Tajifar, “Low-Power Low-Noise Integrated Circuit for Sensign and Driving AMR-based Three Axis Magnetometers” Master Thesis, 2015, advisor **Prof. Andrea Bonfanti**, co-advisor Dr. Stefano Brenna, Politecnico di Milano
- Francesco Lazzarini, Michele Suraci, “Sistema integrato di acquisizione ed elaborazione di segnali neuronali per la terapia del morbo di Parkinson tramite Adaptive Deep Brain Stimulation”,Master Thesis, 2015, advisor **Prof. Andrea Bonfanti**, co-advisor Dr. Stefano Brenna, Politecnico di Milano.
- Mauro Leoncini, “Tecnica di analisi spettrale di un PLL basata su macro-modelli tempo-varianti parametrici” Master Thesis, 2016, advisor Prof. Salvatore Levantino, co-advisor **Prof. Andrea Bonfanti**, Politecnico di Milano.

UNDERGRADUATE THESIS

- Andrea Bianchini, “Soluzione ibrida analogico-digitale per la sintesi di frequenza in applicazioni wireless”, Undergraduate Thesis, 2003, advisor Prof. Andrea Lacaita, co-advisor **Ing. Andrea Bonfanti**, Politecnico di Milano.
- Marco Binda, “Effetti del degrado da portatori caldi nei circuiti a radio-frequenza”, Undergraduate Thesis, 2003, advisor Prof. Andrea Lacaita, co-advisor **Ing. Andrea Bonfanti**, Politecnico di Milano.

PUBLICATIONS

- **Papers in international journals**

[1] S. Levantino, C. Samori, **A. Bonfanti**, S. Gierkink, A. L. Lacaita, "Frequency Dependence on Bias Current in 5-GHz CMOS VCO’s: Impact of Tuning Range and Flicker Noise Up-conversion”, *IEEE*

Journal of Solid State Circuits, pp. 1003-1011, vol. 37, n° 8, August 2002. DOI: 10.1109/JSSC.2002.800969

[2] P. Andreani, **A. Bonfanti**, L. Romanò, C. Samori, "Analysis and Design of a 1.8GHz CMOS LC Quadrature VCO", *IEEE Journal of Solid State Circuits*, pp. 1737-1747, vol. 37, n° 12, Dec. 2002, DOI: 10.1109/JSSC.2002.804352

[3] **A. Bonfanti**, F. Amorosa, C. Samori, A. L. Lacaita, "A DDS-based PLL for 2.4-GHz frequency synthesis", *IEEE Transaction on Circuits and Systems II - Express Briefs*, pp. 1007-1010, vol. 50, n° 12, Dec.r 2003, DOI: 10.1109/TCSII.2003.820250

[4] S. Levantino, **A. Bonfanti**, L. Romanò, C. Samori, A. L. Lacaita, "Differentially-Tuned VCO with Reduced Tuning Sensitivity and Flicker Noise Up-Conversion", *Analog Integrated Circuits and Signal Processing*, Vol. 42, n°1, pp. 21-29, KLUWER Academic, DOI: 10.1007/s10470-004-6844-0

[5] **A. Bonfanti**, A. Tedesco, C. Samori, A. L. Lacaita, "A 15-GHz Broad-Band ÷2 Frequency Divider in 0.13-µm CMOS for Quadrature Generation", *IEEE Microwave and Wireless Components Letters*, pp. 724-726, vol. 15, n° 11, November 2005. DOI: 10.1109/LMWC.2005.858997

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Milano, 12/12/2016

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