Curriculum Vitæ et Studiorum

Vincenzo Rana

Personal Data

Name Vincenzo

Surname Rana

Date of Birth July 8th, 1982

Place of Birth Milan - Italy

Nationality Italian

Marital Status Single

Fiscal Code RNAVCN82L08F205Y

Contacts

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Main Information

Research Interests The research interests of Vincenzo Rana span from the definition and the design of **efficient and high-performance hardware architectures** to the development and optimization of **computationally intensive algorithms for data analysis** in different application fields.

On the one hand, in fact, he has worked on several **advanced heterogeneous computing architectures**, such as dynamically reconfigurable multi-core SoCs and multi-FPGAs clustered architectures. He mainly focused on data memory management, optimal multi-processor SoC communication and efficiency/performance issues. He also faced the design, the development and the programming of custom **efficient and high-performance hardware systems for computationally intensive algorithms**, such as parallel and pipelined hardware implementations for regular expression matching and complex multimedia algorithms. Finally, he also explored the possibility of designing computing platforms combining hardware reconfiguration and adaptive computation for image processing applications.

On the other hand, he worked on the development of **machine learning and big data analysis algorithms** applied to different real-time environments, such as in-vitro neural networks analysis and public transport service optimization. For what concerns this last field, his effort has been twofold: the reconstruction of public transport state, along with user context estimation, for intelligent service scheduling and the accurate prediction of traffic flows by applying knowledge discovery and data mining techniques to car sharing data. Finally, he exploited **deep learning and artificial neural network techniques** to develop an embedded and wearable system able to identify the emotional state of a patient by analyzing his/her physiological signals.

Publications Vincenzo Rana has published **59 papers on international journals and conferences** and **6 book chapters**. Among these publications, some have achieved resounding success within the international scientific community, such as:

- the journal paper *Island-Based Adaptable Embedded System Design* published in the *Embedded Systems Letters (ESL)* journal, which has been for 6 months (from March to August 2011) among the 5 most read *ESL* papers (for 3 months at the first place);
- the paper *Design Exploration of Energy-Performance Trade-Offs for Wireless Sensor Networks* published at *DAC 2012*, which has been the winner of the HiPEAC Paper Award;
- the paper *A high-level synthesis flow for the implementation of iterative stencil loop algorithms on FPGA devices* published at *DAC 2013*, which has been selected among the 8 best papers (over more than 800 submissions) of the *DAC 2013* conference and nominated for the *Best Paper Award*.

The total number of citations achieved by all the papers published by Vincenzo Rana is **533** (380 in the last 5 years), his *h-index* is **13** and his *i10-index* **16**.

Scientific Activities Vincenzo Rana has been the *local chair* of the conference *Great Lakes Symposium on VLSI (GLSVLSI) 2011* and *Conference on Field Programmable Logic (FPL) 2010*, and he has been a member of the *program committee* of several international conferences, such as *Conference on Field Programmable Logic* (FPL) and *Design, Automation, and Test in Europe Conference* (DATE). Since 2008 he is a member of HiPEAC Reconfigurable Computing Cluster.

Research Projects Vincenzo Rana has been the **project leader** of several international research projects (for a total of over **700 k€** in the last few years):

- from 2014 to 2015 he has devised and supervised as *project leader* the project entitled *Support for the definition of a management system for the optimization of energy efficiency in complex buildings* (∼**50 k€**) in collaboration with SIEMENS;
- from 2011 to 2013 he has been the *project leader* of the project entitled *Design of a Wearable Dysphagia Analysis System* (∼**370 k€**), in collaboration with **École Polytechnique Fédérale de Lausanne (EPFL)** and **NRC (Nestlé Research Center)**;
- from 2010 to 2012 he has devised, together with Prof. David Atienza (EPFL), and then supervised as *project leader* the project entitled *Dynamically Adaptive Architectures for Nomadic Embedded Systems* (∼**300 k€**), funded by **SNSF** (Swiss National Science Foundation);
- in 2008 he has devised and carried on the project entitled *A novel design flow for FPGA- based systems based on 2D reconfigurable Networks-on-Chip* (**5 k€**) and in 2009 the project entitled *Dynamically Adaptive Architectures for Nomadic Embedded Systems* (**5 k€**), both result of a collaboration between *Politecnico di Milano* and *EPFL* and funded by the *European Network of Excellence on High Performance and Embedded Architecture and Compilation* (HiPEAC Network).

Among the other projects in which Vincenzo Rana has been involved in the last few years it is possible to find **MOKA**, a travel assistant for the optimization of public transportation in the urban area of Milan, and **CodeLab**, a web-based platform for the online development, compilation and execution of code (C, Python, JavaScript, etc.) in a cooperative and collaborative fashion.

Teaching Activities Vincenzo Rana is the lecturer of the course **Informatica Applicata** (*Laboratorio di Computer Grafica*) targeting bachelor students of *Design della Comunicazione* at Politecnico di Milano, for the academic years 2016/2017 and 2017/2018. He has also been the lecturer of the **MOOC** *Coding - il linguaggio nascosto delle cose*, realized together with Prof. Francesco Bruschi in 2016. He has also been the teacher of several programming courses (*Python*, *C*, *C++*)

targeting employees of C.E.M.B. S.p.A. and students of different high-school institutes, such as Vittorio Veneto, Alessandro Volta, Severi Correnti and Cesare Beccaria. Vincenzo Rana has been co-teacher, with Prof. David Atienza (EPFL), of **2** editions of the Ph.D.course **Co-design of Systems-on-Chip on Reconfigurable Hardware**, in the academic years 2010/2011 and 2012/2013. Since 2006, he has co-supervised several students (**17** bachelor students, **20** master students and **9** Ph.D. students) of both Politecnico di Milano and EPFL.

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1 Personal Data, Education and Service Record

1.1 Current Position

Vincenzo Rana is currently a **Post-Doc** at *Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB)* of Politecnico di Milano. He actively collaborates from March 2010 with Prof. Donatella Sciuto within the *Novel and Emerging Computing System Technologies Laboratory (NECST Lab)* of Politecnico di Milano.

Since 03/2010 **Post-Doc** at Politecnico di Milano (DEIB - Prof. Donatella Sciuto) [Milan, Italy]

1.2 Academic Curriculum

9/2014 - 2/2015 **Project Leader** of the project *Support for the definition of a management system for the optimization of energy efficiency in complex buildings* (∼50 k€) in collaboration with SIEMENS [Milan, Italy]

11/2011 - 7/2013 **Project Leader** of the project entitled *Design of a Wearable Dysphagia Analysis System* in collaboration with **École Polytechnique Fédérale de Lausanne (EPFL)** and **NRC (Nestlé Research Center)** [Lausanne, Switzerland]

04/2010 - 7/2013 **Research Associate** at **EPFL** (ESL - Prof. David Atienza) - **double affiliation** resulting from a collaboration between Politecnico di Milano and EPFL [Lausanne, Switzerland]

03/2010 - 02/2012 **Project Leader** of the project entitled *Dynamically Adaptive Architectures for Nomadic Embedded Systems* funded by **SNSF** (Swiss National Science Foundation) [Lausanne, Switzerland]

11/2007 - 03/2010 **Research Associate** at **EPFL** (ESL - Prof. David Atienza, LSI - Prof. Giovanni De Micheli) - visiting period of the **European Ph.D.** at EPFL [Lausanne, Switzerland]

03/2007 - 12/2007 **Collaborator** of the projects PoliLab and PoliCollege, oriented to elementary and intermediate school students - Politecnico di Milano, Polo di Como [Milan, Italy]

01/2007 - 12/2009 Information Engineering **Ph.D. student** at Dipartimento di Elettronica ed Informazione of Politecnico di Milano [Milan, Italy]

01/2007 - 8/2008 **Research Assistant** (Research Title: Architetture NoC riconfigurabili per sistemi embedded basati su FPGA) at Dipartimento di Elettronica e Informazione of Politecnico di Milano [Milan, Italy]

10/2006 - 12/2006 **Research Assistant** (Research Title: Esplorazione a livello di sistema per la progettazione di piattaforme MPSoC riconfigurabili) at Dipartimento di Elettronica e Informazione of Politecnico di Milano [Milan, Italy]

3/2006 - 7/2006 **Research Assistant** at **Heinz Nixdorf Institut (HNI)**, Universität Paderborn [Paderborn, Germany]

1.3 Language Skills

Italian Native Speaker

English Excellent

French Good

1.4 Education

Vincenzo Rana received his Laurea Specialistica *cum laude* in Computer Engineering in 2006 and his European Ph.D. *cum laude* in Information Engineering in 2010 from Politecnico di Milano, Italy.

March 2010 **European Ph.D.** (Doctorate) *cum laude* in Information Engineering
Dipartimento di Elettronica e Informazione, Politecnico di Milano
Major Thesis:
- Title: NoC-based Reconfigurable Embedded Systems Design
- Advisor: Prof. Donatella Sciuto
- Co-advisor: Prof. Marco D. Santambrogio
- Evaluation: Excellent (A)

Minor Thesis:
- Title: Low Cost Smartcams
- Advisor: Prof. Andrea Bonarini
- Co-advisor: Prof. Matteo Matteucci
- Evaluation: Excellent (A)

Tutor: Prof. Fabrizio Ferrandi

October 2006 **MSc in Computer Engineering**
Politecnico di Milano
Final Grade: 110/110 *cum laude*
Thesis:
- Title: A Novel Methodology for Dynamically Reconfigurable Embedded Systems Design
- Advisor: Prof. Donatella Sciuto
- Co-advisor: Prof. Marco D. Santambrogio

July 2004 **Laurea Degree (B.S. equivalent) in Computer Engineering**
Politecnico di Milano
Final Grade: 110/110 *cum laude*
Thesis:
- Title: Sviluppo di componenti per sistemi dedicati tramite EDK: il caso della DFT
- Advisor: Prof. Fabrizio Ferrandi
- Co-advisor: Prof. Marco D. Santambrogio

1.5 Stays Abroad

In the last few years, Vincenzo Rana has performed his research activities in collaboration with several research groups, such as the *Integrated System Laboratory* (LSI) of Giovanni De Micheli (EPFL) and the *Embedded System Laboratory* (ESL) of David Alonso Atienza (EPFL), and prestigious universities or research institutes, such as Northwestern University, Heinz Nixdorf Institut and Universität Paderborn.

- **École Polytechnique Fédérale de Lausanne (EPFL)**
  November 2007 - July 2013
- **Heinz Nixdorf Institute (HNI) - Universität Paderborn**
  March - July 2006

1.6 General Information

Since 2008 Member of HiPEAC, European Network of Excellence on High Performance and Embedded Architecture and Compilation

Since 2008 Member of HiPEAC Reconfigurable Computing Cluster

2 Scientific Activities

2.1 Research Fields

The main research area of Vincenzo Rana is the design of **high-performance embedded systems**. In particular, his research interests involve embedded systems design methodologies and architectures ([**A.2**], [**A.3**], [**A.6**], [**A.7**], [**C.1**], [**C.17**], [**C.31**], [**C.39**], [**C.40**], [**C.42**], [**C.43**]), reconfigurable systems ([**B.1**], [**C.2**], [**C.3**], [**C.4**], [**C.6**], [**C.7**], [**C.8**], [**C.9**], [**C.10**], [**C.11**], [**C.13**], [**C.18**], [**C.20**], [**C.28**], [**D.2**]), the design and the optimization of communication infrastructures ([**B.2**], [**B.3**], [**B.4**], [**B.5**], [**B.6**], [**C.12**], [**C.14**], [**C.16**], [**C.19**], [**C.21**], [**C.25**], [**C.27**], [**C.32**]), the mapping and scheduling for reconfigurable communication infrastructures ([**A.1**], [**A.4**], [**C.22**], [**C.23**], [**C.24**], [**C.26**], [**C.33**]), operating system supports for run-time reconfigurability ([**C.15**], [**C.5**], [**C.29**]), quantum computing, the definition of models and the optimization of wireless and body sensor networks ([**C.34**], [**C.35**], [**C.36**], [**C.37**], [**C.38**]), the definition of smart spaces for energy consumption management ([**C.41**], [**C.44**], [**C.45**], [**C.46**], [**C.47**]), the design of embedded systems for multimedia and 3D reconstruction and the definition of novel technologies for the optimization of public and private transportation ([**A.5**], [**C.48**], [**C.48**], [**C.50**], [**C.51**], [**C.52**]).

2.1.1 Embedded Systems Design

In addition to the definition of tools for the generation of hardware modules for Xilinx FPGA [**C.1**] and of novel architectures for embedded systems [**A.2**], Vincenzo Rana has implemented a vision system able to recognize, classify and track moving objects [**C.17**] and has collaborated to the design of an innovative high-performance system [**C.31**] able to execute in real-time the Chambolle algorithm on FPGA devices. This algorithm belongs to the class of *Iterative Stencil Loop (ISL)* algorithms, which are commonly used in several real-world applications (e.g., to implement automatic image processing tasks, through the estimation of the *optical flow*). Thanks to the observations made while implementing the optimized architecture for the Chambolle algorithm, Vincenzo Rana has been able to define an innovative methodology for the high level synthesis and the automatic parallelization of ISL algorithms ([**A.3**], [**C.39**], [**D.7**], [**A.6**], [**A.7**]), which has achieved resounding success within the international scientific community.

2.1.2 Dynamic Reconfigurability

The analysis and the study performed by Vincenzo Rana on reconfigurable systems and on the methodologies for their design ([**C.6**], [**C.10**]) have highlighted several critical issues that negatively affect the design, optimization and commercialization of this kind of systems. Among these issues, which have been successfully addressed by Vincenzo Rana in the last few years, it is possible to find the definition of a methodology for the automatic generation of hardware modules for reconfigurable architectures ([**C.2**], [**D.2**]), the dynamic allocation of these modules on the reconfigurable slots ([**B.1**], [**C.4**], [**C.8**]), the definition of a reconfiguration controller able to manage all the reconfiguration-related tasks [**C.11**] and the dynamic management of the memory during reconfiguration processes ([**C.7**], [**C.13**]).

Thanks to this work, Vincenzo Rana has been able to realize several reconfigurable embedded systems, such as the one able to execute in real-time the cyphering and decyphering of data [**C.20**], the one for the automatic matching of regular expressions [C19] or the one for the real-time elaboration of audio streams [**C.18**].

Finally, Vincenzo Rana has explored with great success the possibility of combining hardware dynamic reconfigurability with adaptive software computation techniques ([**C.3**], [**C.9**]).

Communication Infrastructures The main results of the work performed by Vincenzo Rana in the field of reconfigurable communication infrastructures have been the creation of a well known design framework, named *Communication Infrastructure Tailored to Embedded Systems (CITiES)* ([**B.2**], [**B.5**], [**C.12**], [**C.16**], [**C.21**], [**C.27**], [**D.3**], [**D.5**]) and the definition of a novel communication infrastructure, based on the

Network-on-Chip paradigm, optimized for reconfigurable systems ([**B.3**], [**B.4**], [**B.6**], [**C.14**], [**C.19**], [**C.25**], [**D.4**]), in addition to the development of tools for the dynamic management or network resources and the validation of their behaviour [**C.32**].

Mapping and Scheduling In order to exploit the potential of reconfigurable communication infrastructures, Vincenzo Rana has faced the problem of the minimization of reconfiguration timing overheads [**C.22**], needed to perform the dynamic mapping and scheduling of applications, which can vary at run-time depending on the status of the system, on the surrounding environment and on the users requirements. In this context, Vincenzo Rana has collaborated to the definition of a novel mapping flow ([**A.1**], [**A.4**], [**C.24**], [**C.26**]), of a novel algorithm for the scheduling and the 2D placement [**C.23**] of these applications, and of a hybrid mapping-scheduling technique [**C.33**].

Operating Systems Support The implementation of Operating System supports able to transparently handle reconfiguration processes ([**C.15**], [**C.29**]) has been a key factor for the development of portable and reusable code for reconfigurable embedded systems. For instance, the main goal of the work presented in [**C.5**] has been the integration of a dynamic reconfiguration controller and of all its kernel modules within a specific version of the Linux Operating System.

2.1.3 Quantum Computing

The output of the work performed by Vincenzo Rana on quantum computing (*Quantum-Dot Cellular Automata (QCA)*) has been the development of an adder [**C.30**], implemented following the QCA logic rules, with a higher efficiency with respect to the ones available in the state of the art, in terms of ratio between required resources and computation latency.

2.1.4 Sensor Networks

Vincenzo Rana has actively collaborated to the definition of models for the design of *Wireless Body Sensor Networks (WBSN)* [**C.34**], to the development of techniques for the reduction of the interferences among co-located sensor networks [**C.35**] and to the study of the trade-offs between performance and energy consumption ([**C.36**], [**C.37**], [**C.38**]).

2.1.5 Energy efficiency

Vincenzo Rana has contributed to the creation of a simulation [**C.41**] and analysis ([**C.44**], [**C.46**], [**C.47**]) framework for the energy efficiency of *smart spaces*. He also has collaborated to the realization of a system able to estimate room occupancy thanks to the *iBeacon* technology [**C.45**].

2.1.6 Multimedia Systems

Vincenzo Rana has been the project leader of the *MatraCam* project, carried out in collaboration with the *MetaMedia Center* (MMC) of the EPFL, aiming at studying, designing and realizing a vision system able to perform 3D reconstruction of images and video, which has been used to record live events during the *Montreux Jazz Festival* in 2011 and 2012.

2.1.7 Neural Networks

Vincenzo Rana has contributed to the development, in collaboration with the *Università degli Studi di Milano-Bicocca*, of the *Neuron On Network (NeON)* tool, able to automatically analyze and visualize (starting from the information on the neurons spikes gathered with MultiElectrod Array, MEA, devices) the structure of *in vitro* neural networks, aiming at supporting the study of illness such as epilepsy and Alzheimer's disease.

2.2 Organization Activities

Vincenzo Rana has actively contributed to the creation of the *Dynamic Reconfigurability in Embedded Systems Design* (DRESD) research group and he is a co-founder of the *iDRESD* association. Among the projects he is currently managing, it is possible to find:

- **MOKA Travel Assistant**
  MOKA [**A.5**] is an experimental Travel Assistant that supports people while moving with the public transit of Milan. In particular, MOKA is able to:
  - elaborate a set of paths that allow to move with the public transit between two points of Milan
  - calculate the estimated travel time, keeping into account all the needed connections (thus evaluating the possibility of a missed connection)

  During the travel, MOKA keeps the user continuously updated about:
  - estimated time of arrival
  - information coming (e.g., tweet) from Azienda Trasporti Milanesi (ATM)
  - informazioni coming from other users (e.g., facebook, twitter)
  - current position of the user (in order to evaluate, for instance, how many stops still have to be covered before reaching the destination)
- **CODELAB**
  Codelab is a system that allow to write, compile and execute C code through a web site, keeping into account both cooperation and collaboration. In particular, Codelab is used within the course *Fondamenti di Informatica* of Politecnico di Milano to teach C programming and to evaluate the programming skills acquired by the students of the course.

2.2.1 Research Projects

Vincenzo Rana has devised and supervised as **project leader**, from September 2014 to February 2015, a project for the definition of a management system for the optimization of the energy efficiency of complex buildings, as a collabaration between **Politecnico di Milano** and **SIEMENS**.

From November 2011 to July 2013 he has supervised as **project leader**, within a collaboration between **École Polytechnique Fédérale de Lausanne** (EPFL) and **Nestlé Research Center** (NESTEC), a research project for the design and the development of a wearable system for the detection and the analysis of dysphagia, a condition in which disruption of the swallowing process interferes with the ability to eat, possibly resulting in aspiration pneumonia, malnutrition, dehydration, weight loss, and airway obstruction.

Finally, from March 2010 to February 2012 he has been the **project leader** at **École Polytechnique Fédérale de Lausanne** of a project funded by SNSF (**Swiss National Science Foundation**) and dealing with dynamically adaptive architectures for nomadic embedded systems.

- Collaboration between **Politecnico di Milano** and **SIEMENS**:
  Support for the definition of a management system for the optimization of energy efficiency in complex buildings
  Budget: ∼**50 k€**
  Date: September 2014 - February 2015
- Collaboration between **EPFL** and **NRC** (Nestlé Research Center):
  Design of a Wearable Dysphagia Analysis System
  Budget: ∼**370 k€**
  Date: November 2011 - July 2013
- **SNSF** (Swiss National Science Foundation) project:
  Dynamically Adaptive Architectures for Nomadic Embedded Systems
  Budget: ∼**300 k€**
  Date: March 2010 - February 2012

2.2.2 Organization of international conferences

Vincenzo Rana has been the *local chair* of the conference *Great Lakes Symposium on VLSI (GLSVLSI) 2011* and *Conference on Field Programmable Logic (FPL) 2010*, and he has been a member of the *program committee* of several international conferences, such as *Conference on Field Programmable Logic* (FPL) and *Design, Automation, and Test in Europe Conference* (DATE). Since 2008 he is a member of HiPEAC Reconfigurable Computing Cluster.

- **Organizer** of the conference *Great Lakes Symposium on VLSI*
  Date: 2-4 May 2011
  Place: EPFL, Lausanne (Switzerland)
  Role: Local Chair
- **Organizer** of the *Conference on Field Programmable Logic*
  Date: August 31st - September 2nd 2010
  Place: Politecnico di Milano, Milan (Italy)
  Role: Local Chair

2.2.3 Organization of national workshops and seminars

- *Partial Dynamic Reconfiguration Workshop*, at Nokia Siemens Networks in Cinisello Balsamo, Milan, April 23rd, 2008
- *Reconfigurable Computing Italian Workshop*, at Politecnico di Milano, Milan, Dicember 19th, 2008

2.2.4 Technical Program Committee (TPC)

- Workshop on Reconfigurable Computing (WRC) 2014
- Conference on Parallel, Distributed and Network-Based Computing (PDP) 2014
- Reconfigurable Architectures Workshop (RAW) 2013, 2014, 2015
- Design, Automation, and Test in Europe Conference (DATE) 2012, 2013, 2014
- Conference on Embedded and Ubiquitous Computing (EUC) 2011, 2012, 2013
- Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHA'N'GE) 2011, 2012
- Conference on Design and Architectures for Signal and Image Processing (DASIP) 2011
- Conference on Field Programmable Logic (FPL) 2010, 2011, 2012, 2013, 2014

2.2.5 National and International Collaborations

In the last few years, Vincenzo Rana has established several fruitful collaborations with prestigious universities and companies, such as *Northwestern University (NU)*, *École Polytechnique Fédérale de Lausanne (EPFL)*, *Massachusetts Institute of Technology (MIT)*, *ST Microelectronics* and *Nestlé Research Center (NRC)*, cooperating with them to numerous research projects and developing innovative embedded systems.

- Universities:
  - *Politecnico di Milano* - Milan, Italy
  - *Università Statale di Milano* - Milan, Italy
  - *Università degli Studi di Milano-Bicocca* - Milan, Italy
  - *Università di Paderborn* - Paderborn, Germany
  - *Northwestern University (NU)* - Evanston, Illinois, USA
  - *University of Westminster* - London, UK
  - *Imperial College* - London, UK
  - *École Polytechnique Fédérale de Lausanne (EPFL)* - Lausanne, Switzerland

  - *Massachusetts Institute of Technology (MIT)* - Cambridge, MA, USA

- Companies:
  - *ST Microelectronics* - Milan, Italy
  - *Heinz Nixdorf Institut (HNI)* - Paderborn, Germany
  - *Sony Computer Entertainment Europe (SCEE)*
  - *Inpeco* - Lugano, Switzerland
  - *Nestlé Research Center (NRC)* - Lausanne, Switzerland
  - *Azienda Trasporti Milanesi (ATM)* - Milan, Italy
  - *Telecom* - Italy
  - *Agenzia Mobilità Ambiente Territorio (AMAT)* - Milan, Italy
  - *Deloitte* - Milan, Italy
  - *Finmeccanica* - Rome, Italy
  - *SIEMENS* - Milan, Italy
  - *Chinesport S.p.A.* - Udine, Italy
  - *Startec S.r.l.* - Sesto al Reghena, Italy
  - *Saipem S.p.A.* - San Donato Milanese, Italy

- Main collaborations:

2017 *L. Sut* and *Avv. A. Dario* - Technical expert for legal issues (CTP) for **Startec S.r.l.**, Italy

2017 *T. Persello* and *Avv. A. Dario* - Technical expert and consultant for legal issues for **Chinesport S.p.A.**, Italy

2016-2017 *M. Caon* - Technical expert and consultant for **Saipem S.p.A.**, Italy

2008-2016 *Avv. G. Casucci*, *Avv. M. Casucci*, *Avv. G. Muscas* and *Avv. R. Castiglioni* - Technical expert for legal issues (CTP) for **Sony Computer Entertainment Europe (SCEE)**, Italy

2010-2015 *D. Atienza* - Dynamically Adaptive Architectures for Nomadic Embedded Systems, **École Polytechnique Fédérale de Lausanne** (ESL), Swiss

2013-2014 Technical expert and consultant for **Deloitte** and **Finmeccanica**, Italy

2014 *M. Bigoloni* - Support for the definition of a management system for the optimization of energy efficiency in complex buildings, for **EXPO2015** with **SIEMENS**, Italy

2012-2014 *E. Wanke* - Automatic analysis of neural networks data, **Università degli Studi di Milano-Bicocca**, Italy

2010-2013 *D. Atienza* - Design of a Wearable Dysphagia Analysis System, **École Polytechnique Fédérale de Lausanne** and **NRC (Nestlé Research Center)**, Swiss

2007-2012 *G. De Micheli* - Reconfigurable NoC architectures, **École Polytechnique Fédérale de Lausanne** (LSI), Swiss

2006-2009 *S. Ogrenci Memik* - Adaptive computation and scheduling/placement heuristics, **Northwestern University (NU)**, USA

2008 *D. Caltabiano e R. Sannino* - Low cost smartcams design, **STMicroelectronics**, Italy

2006 *M. Porrmann e U. Rückert* - Partial dynamic reconfiguration in a multi-FPGAs clustered architecture based on Linux, **Heinz Nixdorf Institut (HNI)** and **Universität Paderborn**, Germany

2.3 Reviewer Activities

2.3.1 Journals

- IEEE Transactions on Computer-Aided Design (TCAD)
- IEEE Transactions on Parallel and Distributed Systems (TPDPS)
- IEEE Embedded Systems Letters (ESL)
- IEEE Transactions on Industrial Informatics (TII)
- ACM Transaction on Reconfigurable Technology and Systems (TRETS)
- ACM Transactions on Embedded Computing Systems (TECS)
- Journal of Systems Architecture (JSA) - Elsevier
- Integration, the VLSI Journal - Elsevier
- Computer & Electrical Engineering - Elsevier

2.3.2 Conferences

- International Symposium on Applied Reconfigurable Computing (ARC)
- IEEE Design Automation Conference (DAC)
- IEEE Design, Automation and Test in Europe (DATE)
- IEEE International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)
- IEEE International Conference on Field Programmable Logic and Applications (FPL)
- IEEE Reconfigurable Architectures Workshop (RAW)
- IEEE Computer Annual Symposium on VLSI (ISVLSI)
- Southern Conference on Programmable Logic (SPL) Conference
- IEEE Field Programmable Technology (FPT)
- ACM Great Lake Symposium VLSI (GLSVLSI)
- International Symposium on System-on-Chip (SoC)
- IFIP International Conference on Very Large Scale Integration (VLSI-SoC)
- International Conference on ReConFigurable Computing and FPGAs (ReConFig)
- IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC)

3 Teaching Activities

Vincenzo Rana is the lecturer of the course **Informatica Applicata** (*Laboratorio di Computer Grafica*) targeting bachelor students of *Design della Comunicazione* at Politecnico di Milano, for the academic years 2016/2017 and 2017/2018. He has also been the lecturer of the **MOOC** *Coding - il linguaggio nascosto delle cose*, realized together with Prof. Francesco Bruschi in 2016. He has also been the teacher of several programming courses (*Python*, *C*, *C++*) targeting employees of C.E.M.B. S.p.A. and students of different high-school institutes, such as Vittorio Veneto, Alessandro Volta, Severi Correnti and Cesare Beccaria. Vincenzo Rana has been co-teacher, with Prof. David Atienza (EPFL), of **2** editions of the Ph.D.course **Co-design of Systems-on-Chip on Reconfigurable Hardware**, in the academic years 2010/2011 and 2012/2013.

3.1 Teacher

- Course: *Informatica Applicata (Laboratorio di Computer Grafica)*
  Target: bachelor students (Design della Comunicazione)
  Teacher: Vincenzo Rana
  Place: Politecnico di Milano
  Academic years: 2017/2018, 2016/2017
- Course: *Python per creatori di mondi*
  Target: high-school
  Teachers: Vincenzo Rana and Francesco Bruschi
  Place: IIS Severi Correnti
  Date: 2017, 2016
- Course: *Street Fighting Python*
  Target: high-school students
  Teachers: Vincenzo Rana and Francesco Bruschi
  Place: Liceo Scientifico Alessandro Volta
  Date: 2017, 2016
- Course: *Street Fighting Python*
  Target: high-school
  Teachers: Vincenzo Rana and Francesco Bruschi
  Place: Liceo Scientifico Vittorio Veneto
  Date: 2017, 2016
- Course: *Programmazione C, C++ e strumenti di automazione*
  Target: CEMB S.p.A. employees
  Teachers: Vincenzo Rana and Francesco Bruschi
  Place: CEMB S.p.A. (*http://www.cemb.com*)
  Date: December 2015 - March 2016
- Course: *Coding - il linguaggio nascosto delle cose*
  Target: italian citizens
  Teachers: Vincenzo Rana and Francesco Bruschi
  Type: Massive Open Online Course (MOOC) of the Politecnico di Milano
  Date: February - March 2016
- Course: *Co-design of Systems-on-Chip on Reconfigurable Hardware*
  Target: Ph.D. students
  Teachers: Vincenzo Rana and Prof. David Atienza
  Place: École Polytechnique Fédérale de Lausanne
  Academic years: 2012/2013, 2010/2011

3.2 Teaching assistant

- Teaching assistant activities at Politecnico di Milano (Milan, Italy)
  - Course: High Performance Processors and Systems
    Target: master students (english lessons)
    Prof.: Donatella Sciuto
    Academic year: 2008/2009

  - Course: Architettura dei Calcolatori
    Target: master students
    Prof: Donatella Sciuto
    Academic year: 2009/2010

  - Course: Fondamenti di Informatica
    Target: bachelor students
    Prof: Francesco Bruschi
    Academic year: 2015/2016, 2014/2015, 2013/2014, 2012/2013

  - Course: Fondamenti di Informatica
    Target: bachelor students
    Prof: Daniele Braga
    Academic year: 2017/2018, 2016/2017, 2015/2016

- Teaching assistant activities at Polo di Como of Politecnico di Milano (Como, Italy)

  - Course: Reti Logiche
    Target: bachelor students
    Prof: Francesco Bruschi
    Academic years: 2017/2018, 2016/2017, 2015/2016, 2014/2015, 2013/2014, 2012/2013, 2011/2012, 2010/2011, 2009/2010

  - Course: Architettura dei Calcolatori e Sistemi Operativi
    Target: bachelor students
    Prof: Roberto Negrini
    Academic years: 2017/2018, 2016/2017, 2015/2016, 2014/2015, 2013/2014, 2012/2013, 2011/2012, 2010/2011, 2009/2010

  - Course: Informatica II
    Target: bachelor students
    Prof: Roberto Negrini
    Academic years: 2008/2009, 2007/2008

  - Course: Tecnologia delle informazioni in rete
    Prof: Maurizio Dècina
    Academic year: 2006/2007

- Teaching assistant activities at Università degli Studi di Milano (Crema, Italy)

  - Course: Architettura dei Calcolatori
    Prof: Nello Scarabottolo
    Academic years: 2009/2010, 2008/2009, 2007/2008, 2006/2007

3.3 Lab Teaching Activities

- Laboratory responsible and teaching assistant at Politecnico di Milano (Milan, Italy)

  - Course: Fondamenti di Informatica
    Target: bachelor students
    Prof: Francesco Bruschi
    Academic years: 2015/2016, 2014/2015, 2013/2014, 2011/2012, 2010/2011

  - Course: Informatica
    Target: bachelor students
    Prof: Fausto Distante
    Academic year: 2006/2007

  - Course: Informatica
    Target: bachelor students
    Prof: Francesco Bruschi
    Academic years: 2006/2007, 2005/2006

– Course: Informatica
  Target: bachelor students
  Prof: Cristiana Bolchini
  Academic years: 2006/2007, 2005/2006

3.4 Supervision of Students

Since 2006, Vincenzo Rana has **co-supervised** several students of both Politecnico di Milano and EPFL, collaborating with them for the realization of theses and research projects dealing with the definition of models and the optimization of communication protocols for wireless and body sensor networks, the development of reconfigurable communication infrastructures and the definition of techniques and methodologies for the run-time support of reconfiguration processes:

- Co-advisor of **17** bachelor students at *Politecnico di Milano*
- Co-advisor of **20** master students at *Politecnico di Milano*
- Tutor of **9** Ph.D. students at *Politecnico di Milano* and *EPFL*

4 Prizes and Awards

Vincenzo Rana has been awarded, for his master thesis, with both the **Premio di Laurea Accenture** and the **Premio di Laurea del Politecnico di Milano**. He has also been the winner of two **HiPEAC Collaboration Grants**, in 2008 and 2009, supporting two visiting periods at *École Polytechnique Fédérale de Lausanne (EPFL)*.

- **Prized and awards:**
  - **Winner of the HiPEAC Best Paper Award at DAC 2013**
    for the paper *A high-level synthesis flow for the implementation of iterative stencil loop algorithms on FPGA devices*
  - **Winner of the HiPEAC Best Paper Award at DAC 2012**
    for the paper *Design Exploration of Energy-Performance Trade-Offs for Wireless Sensor Networks*
  - **Third place at "2nd MEMOCODE Hardware/Software Co-Design Contest", 2008**
    Sixth ACM-IEEE International Conference on Formal Methods and Models for Codesign
  - **Winner of the "Premio di Laurea del Politecnico di Milano", 2007**
    for his master thesis
  - **Winner of the "Premio di Laurea Accenture", 2nd edition, 2006**
    for his master thesis

- **Funds:**
  - **Swiss NSF Research Project (Division II), 2010 - 2012**
    Project title: *Dynamically Adaptive Architectures for Nomadic Embedded Systems*
  - **"HiPEAC Collaboration Grant", 2009**
    for the research project entitled: *Dynamically Adaptive Architectures for Nomadic Embedded Systems*
  - **"HiPEAC Collaboration Grant", 2008**
    for the research project entitled: *A novel design flow for FPGA-based systems based on 2D reconfigurable Networks-on-Chip*

5 Publication List

The publications presented in this document are listed in inverse chronological order and are classified according to their typology: Section 5.1 presents the publications on international journals (category **A**), Section 5.2 presents the book chapters (category **B**), Section 5.3 presents publications on international conferences (category **C**), while Section 5.4 presents the publications on international workshops, Ph.D. Forums, Poster Sessions, University Booths and Newsletters (category **D**).

The following index has been computed with *Google Scholar*, considering a total of 65 publications.

- Total number of citations: 533 (380 in the last 5 years)
- *h-index*: 13
- *i10-index*: 16

Among the different publications listed in this document, some have achieved resounding success within the international scientific community, such as:

- the journal paper *Island-Based Adaptable Embedded System Design* published in the *Embedded Systems Letters (ESL)* journal, which has been for 6 months (from March to August 2011) among the 5 most read *ESL* papers (for 3 months at the first place),
- the paper *Design Exploration of Energy-Performance Trade-Offs for Wireless Sensor Networks* published at *DAC 2012*, which has been the winner of the HiPEAC Best Paper Award,
- the paper *A high-level synthesis flow for the implementation of iterative stencil loop algorithms on FPGA devices* published at *DAC 2013*, which has been selected among the best papers of the *DAC 2013* conference and nominated for the *Best Paper Award*.

Regarding the publications realized in collaboration with other authors, since the research has been carried out in strict collaboration with them, the contribution of each one has to be considered equal.

5.1 Publication on International Journals

A.1 I. Beretta, V. RANA, D. A. Atienza, D. Sciuto
A Mapping Flow for Dynamically Reconfigurable Multi-Core System-on-Chip Design
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
Volume 30, Issue 8, August 2011, Pag. 1211-1224
Digital Object Identifier: 10.1109/TCAD.2011.2138140
Society Manuscript Number: TCAD-2011-0147

A.2 I. Beretta, V. RANA, D. A. Atienza, D. Sciuto
Island-Based Adaptable Embedded System Design
IEEE Embedded Systems Letters (ESL)
Volume 3, Issue 2, June 2011, Pag. 53-57
Digital Object Identifier: 10.1109/LES.2011.2115991
Society Manuscript Number: IEEE-ESL-Jul-10-0095

A.3 V. RANA, A. Nacci, I. Beretta, M. D. Santambrogio, D. A. Atienza, D. Sciuto
Design Methods for Parallel Hardware Implementation of Multimedia Iterative Algorithms
IEEE Design & Test of Computers (D&T)
Published by: IEEE Council on Electronic Design and Automation
Digital Object Identifier: 10.1109/MDT.2012.2223191
Society Manuscript Number: DT-2012-01-0013

A.4 J. Clemente, I. Beretta, V. RANA, D. A. Atienza, D. Sciuto
A Mapping-Scheduling Algorithm
for Hardware Acceleration for Reconfigurable Platforms
ACM Transactions on Reconfigurable Technology and Systems (TRETS)
Volume 7, Issue 2, June 2014, Article No. 9, 27 pages
Digital Object Identifier: 10.1145/2611562

A.5 M. Bruglieri, F. Bruschi, A. Colorni, A. Luè, R. Nocerino, V. RANA
A Real-time Information System for Public Transport in Case of Delays and Service Disruptions
Elsevier Transportation Research Procedia (TRPRO)
Volume 10C, September 2015, Pag. 493-502
Digital Object Identifier: 10.1016/j.trpro.2015.09.003

A.6 I. Beretta, V. RANA, A. Akin, A. Nacci, D. A. Atienza, D. Sciuto
Parallelizing the Chambolle Algorithm
for Performance Optimized Mapping on FPGA devices
ACM Transactions on Embedded Computing Systems (TECS)
ACM New York, NY, USA
Volume 15 Issue 3, March 2016
Article No. 44
Digital Object Identifier: 10.1145/2851497

A.7 V. RANA, I. Beretta, F. Bruschi, A. Nacci, D. A. Atienza, D. Sciuto
Efficient Hardware Design Of Iterative Stencil Loops
IEEE Transactions on Computer-Aided Design
of Integrated Circuits and Systems (TCAD)
Print ISSN: 0278-0070
Online ISSN: 1937-4151
Digital Object Identifier: 10.1109/TCAD.2016.2545408

5.2 Books Chapters

B.1 V. RANA, C. Sandionigi, M. D. Santambrogio, D. Sciuto
An adaptive genetic algorithm for dynamically reconfigurable modules allocation
R. Reis, V. Mooney and P. Hasler (Eds.), VLSI-SoC: Advanced Topics on Systems on a Chip, Springer, 2009, Vol. 291, p. 209 - 226

B.2 A. Meroni, V. RANA, M. D. Santambrogio, F. Bruschi
Design of Communication Infrastructures for Reconfigurable Systems
M. Radetzki (Eds.), Languages for Embedded Systems and their Applications Selected Contributions on Specification, Design, and Verification from FDL08, Springer, 2009, Vol. 36, p. 291-307

B.3 V. RANA, D. A. Atienza, M. D. Santambrogio, D. Sciuto, G. De Micheli
A Reconfigurable Network-on-Chip Architecture for Optimal Multi-Processor SoC Communication
D. Soudris, C. Piguet and R. Reis (Eds.), VLSI-SoC: Design Methodologies for SoC and SiP, Springer, 2009, Volume 313, 2010, pp 232-250

B.4 V. RANA, M. D. Santambrogio, S. Corbetta
Dynamic Reconfigurable NoCs: Characteristics and Performance Issues
Jih-Sheng Shen Pao-Ann Hsiung (Eds.), Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication", IGI Global Publisher, 2009

B.5 V. RANA, M. D. Santambrogio, A. Meroni
Design Methodologies and Mapping Algorithms for Reconfigurable NoC-based Systems
Jih-Sheng Shen Pao-Ann Hsiung (Eds.), Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication", IGI Global Publisher, 2009

B.6 V. RANA, F. Bruschi, A. Miele, M. Santambrogio, D. Sciuto
Design Methodologies for Reconfigurable NoC-based Embedded Systems
Pierre-Emmanuel Gaillardon (Eds.), Edited book, Part of the *Devices, Circuits,*

and Systems Series, CRC press, 28 October 2015
ISBN: 9781482262186

5.3 International Conferences

C.1 F. Ferrandi, G. Ferrara, R. Palazzo, V. RANA, M. D. Santambrogio
VHDL to FPGA automatic IPCore generation: A case study on Xilinx design flow
20th IEEE International Parallel and Distributed Processing Symposium (IPDPS 06) - Reconfigurable Architecture Workshop - RAW, proc. p. 219, Isola di Rodi, Grecia, Aprile 2006

C.2 M. Murgida, A. Panella, V. RANA, M. D. Santambrogio, D. Sciuto
Fast IP-Core Generation in a Partial Dynamic Reconfiguration Workflow
14th IFIP International Conference on Very Large Scale Integration - IFIP VLSI-SOC 2006, proc. p. 74 - 79, Nizza, Francia, Ottobre 2006

C.3 V. RANA, S. Ogrenci Memik, M. D. Santambrogio, D. Sciuto
Combining Hardware Reconfiguration and Adaptive Computation for a Novel SoC Design Methodology
International Conference on Field Programmable Technology - FPT 06, proc. p. 293 - 296, Bangkok, Tailandia, Dicembre 2006

C.4 V. RANA, C. Sandionigi, M. D. Santambrogio
A genetic algorithm based solution for dynamically reconfigurable modules allocation
IEEE 3rd Southern Conference on Programmable Logic, SPL 07, proc. p. 183 - 186, Mar del Plata, Argentina, Febbraio 2007

C.5 V. RANA, M. D. Santambrogio, D. Sciuto, D. Kettelhoit, M. Koester, M. Porrmann, U. Rückert
Partial dynamic reconfiguration in a multi-FPGAs clustered architecture based on Linux
21th IEEE International Parallel and Distributed Processing Symposium (IPDPS 07) - Reconfigurable Architecture Workshop - RAW, IEEE online proceedings, Long Beach, California, USA, Marzo 2007

C.6 V. RANA, M. D. Santambrogio, D. Sciuto
Dynamic Reconfigurability in Embedded System Design
IEEE International Symposium on Circuits and Systems, ISCAS 07, proc. p. 2734 - 2737, New Orleans, Louisiana, USA, Maggio 2007

C.7 A. Montone, V. RANA, M. D. Santambrogio
Data memory management in partial dynamically reconfigurable systems
3rd International Conference on Information System Security, ICIIS 07, proc. p. 130, Peradeniya, Sri Lanka, Agosto 2007

C.8 V. RANA, C. Sandionigi, M. D. Santambrogio, D. Sciuto
An adaptive genetic algorithm for dynamically reconfigurable modules allocation
15th International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2007, proc. p. 128 - 133, Atlanta, Georgia, USA, Ottobre 2007
Selezionato tra i migliori lavori presentati alla conferenza, per apparire nel seguente libro: VLSI-SoC: From Systems To Silicon, Springer ([B.1])

C.9 M. D. Santambrogio, V. RANA , S. Ogrenci Memik, D. Sciuto, U. Acar
A Novel SoC Design Methodology Combining Adaptive Software and Reconfigurable Hardware
25th International Conference on Computer-Aided Design, ICCAD 2007, proc. p. 303 - 308, San Josè, California, USA, Novembre 2007

C.10 C. A. Curino, L. Fossati, V. RANA, F. Redaelli, M. D. Santambrogio, D. Sciuto
The Shining embedded system design methodology based on self dynamic reconfigurable architectures
13th Asia and South Pacific Design Automation Conference, ASP-DAC 08, proc. p. 595 - 600, Seoul, Korea, Gennaio 2008

C.11 A. Cuoccio, P. R. Grassi, V. RANA, M. D. Santambrogio, D. Sciuto
A Generation Flow for Self-Reconfiguration Controllers Customization
4th IEEE International Symposium on Electronic Design, Test and Applications, DELTA 08, proc. p. 279 - 284, Hong Kong, Gennaio 2008

C.12 A. Meroni, V. RANA, M. D. Santambrogio, D. Sciuto
A Requirements-Driven Reconfigurable SoC Communication Infrastructure Design Flow
4th IEEE International Symposium on Electronic Design, Test and Applications, DELTA 08, proc. p. 405 - 409, Hong Kong, Gennaio 2008

C.13 A. Montone, V. RANA, M. D. Santambrogio, D. Sciuto
HARPE: a Harvard-based Processing Element Tailored for Partial Dynamic Reconfigurable Architectures
22th IEEE International Parallel and Distributed Processing Symposium (IPDPS 08) - Reconfigurable Architecture Workshop - RAW, IEEE online proceedings, Miami, Florida, USA, Aprile 2008

C.14 S. Corbetta, V. RANA, M. D. Santambrogio, D. Sciuto
A Light-Weight Network-on-Chip Architecture for Dynamically Reconfigurable Systems
IEEE IC-SAMOS 08 - Embedded Computer Systems: Architectures, MOdeling, and Simulation, proc. p. 49 - 56, Samos, Grecia, Luglio 2008

C.15 M. D. Santambrogio, V. RANA, D. Sciuto
Operating System Support for Online Partial Dynamic Reconfiguration Management
18th International Conference on Field Programmable Logic and Applications, FPL 08, proc. p. 455 - 458, Heidelberg, Germania, Settembre 2008

C.16 F. Bruschi, A. Meroni, V. RANA, M. D. Santambrogio
A Requirements-Driven Simulation Framework For Communication Infrastructures Design
FDL 08 - Forum on specification & Design Languages, proc. p. 111 - 117, Stuttgart, Germania, Settembre 2008
Selezionato tra i migliori lavori presentati alla conferenza, per apparire nel seguente libro: VLSI-SoC, Springer ([B.2])

C.17 V. RANA, M. Matteucci, D. Caltabiano, R. Sannino, A. Bonarini
Low cost smartcams design
6th IEEE Workshop on Embedded Systems for Real-time Multimedia - ESTIMedia 2008, proc. p. 27 - 32, Atlanta, GA, USA, Ottobre 2008

C.18 F. Bruschi, V. RANA, D. Sciuto
An Architecture for Dynamically Reconfigurable Real Time Audio Processing Systems
6th IEEE Workshop on Embedded Systems for Real-time Multimedia - ESTIMedia 2008, proc. p. 81 - 86, Atlanta, GA, USA, Ottobre 2008

C.19 V. RANA, D. A. Atienza, M. D. Santambrogio, D. Sciuto, G. De Micheli
A Reconfigurable Network-on-Chip Architecture for Optimal Multi-Processor SoC Communication
International Conference on Very Large Scale Integration, IFIP VLSI-SoC 2008, proc. p. 321 - 326, Isola di Rodi, Grecia, Ottobre 2008
Selezionato tra i migliori lavori presentati alla conferenza, per apparire nel seguente libro: VLSI-SoC, Springer ([B.3])

C.20 I. Beretta, V. RANA, M. D. Santambrogio, D. Sciuto
On-Line Task Management for a Reconfigurable Cryptographic Architecture
23th IEEE International Parallel and Distributed Processing Symposium (IPDPS 09) - Reconfigurable Architecture Workshop - RAW, IEEE online proceedings, Roma, Italia, Maggio 2009

C.21 Dario Cozzi, Claudia Farè, Alessandro Meroni, Vincenzo RANA, M. D. Santambrogio, Dontella Sciuto
Reconfigurable NoC Design Flow for Multiple Applications Run-Time Mapping on FPGA Devices

Great Lake Symposium VLSI, GLSVLSI 09, proc. p. 421 - 424, Boston, Massachusetts, Maggio 2009

C.22 V. RANA, S. Murali, D. A. Atienza, M. D. Santambrogio, L. Benini and D. Sciuto
Minimization of the reconfiguration latency for the mapping of applications on FPGA-based systems
International Conference on Hardware-Software Codesign and System Synthesis, CODESS+ISSS 09, proc. p. 325 - 334, Grenoble, Francia, Ottobre 2009

C.23 F. Redaelli, M. D. Santambrogio, V. RANA, S. Ogrenci Memik
Scheduling and 2D Placement Heuristics for Partially Reconfigurable Systems
International Conference on Field Programmable Technology - FPT 09, proc. p. 223 - 230, Sydney, Australia, Dicembre 2009

C.24 I. Beretta, V. RANA, D. A. Atienza, M. D. Santambrogio, D. Sciuto
Run-time Applications Mapping on Fine-Grained Reconfigurable Embedded Systems
International Conference on Microelectronics - ICM 09, proc. p. 151-154, Marrakech, Marocco, Dicembre 2009
Invited Talk

C.25 V. RANA, M. D. Santambrogio, S. Corbetta, D. Sciuto
Multiple Communication–Domains Design in FPGA–Based Systems–on–Chip
International conference on Design & Technology of Integrated Systems in nanoscale era - DTIS 2010, p. 1 - 6, Hammamet, Tunisia, Marzo 2010

C.26 I. Beretta, V. RANA, D. A. Atienza, D. Sciuto
Run-time Mapping of Applications on FPGA-based Reconfigurable Systems
IEEE International Symposium on Circuits and Systems, ISCAS 10, proc. p. 3329 - 3332, Parigi, Francia, Maggio 2010

C.27 V. RANA, D. Sciuto
A novel design framework for the design of reconfigurable systems based on NoCs
Great Lake Symposium VLSI, GLSVLSI 10, proc. p. 1 - 2, Providence, Rhode Island, USA, Maggio 2010
Invited Paper (Keynote)

C.28 F. Bruschi, M. Paolieri, V. RANA
A Reconfigurable System based on a Parallel and Pipelined solution for Regular Expression Matching
20th International Conference on Field Programmable Logic and Applications, FPL 10, proc. p. 44 - 49, Milano, Italia, Agosto 2010

C.29 M. D. Santambrogio, V. RANA, I. Beretta and D. Sciuto
Operating System Runtime Management of Partially Dynamically Reconfigurable Embedded Systems
IEEE 2010 8th Workshop on Embedded Systems for Real-Time Multimedia - ESTIMedia 2005, proc. p. 1 - 10, Scottsdale, AZ, USA, Settembre 2010

C.30 F. Bruschi, F. Perini, V. RANA, D. Sciuto
An Efficient Quantum-Dot Cellular Automata Adder
Design, Automation and Test in Europe, DATE 11, proc. p. 1220 - 1223, Grenoble, Francia, Marzo 2011

C.31 A. Akin, I. Beretta, A. Nacci, V. RANA, M. D. Santambrogio, D. A. Atienza
A high-performance parallel implementation of the Chambolle algorithm
Design, Automation and Test in Europe, DATE 11, proc. p. 1436 - 1441, Grenoble, Francia, Marzo 2011

C.32 F. Bruschi, A. Miele and V. RANA
On-Chip Network Resource Management Design and Validation
IEEE IC-SAMOS 11 - Embedded Computer Systems: Architectures, MOdeling, and Simulation, proc. p. 249 - 254 , Samos, Grecia, Luglio 2011

C.33 J. Clemente, V. RANA, D. Sciuto, I. Beretta, D. A. Atienza
A Hybrid Mapping-Scheduling Technique for Dynamically Reconfigurable Hardware

21st International Conference on Field Programmable Logic and Applications, FPL 11, proc. p. 177 - 180, Chania, Creta, Grecia, Settembre 2011

C.34 I. Beretta, F. Rincon, N. Khaled, P. R. Grassi, V. RANA, D. A. Atienza
Model-Based Design for Wireless Body Sensor Network Nodes
13th IEEE Latin American Test Workshop, LATW 12, proc. p. 92 - 97, Quito, Ecuador, Aprile 2012

C.35 P. R. Grassi, V. RANA, I. Beretta, Donatella Sciuto
B^2IRS: a Technique to Reduce BAN-BAN Interferences in Wireless Sensor Networks
9th IEEE International Conference on Wearable and Implantable Body Sensor Networks, BSN 2012, proc. p. 46 - 51, Londra, Regno Unito, Maggio 2012

C.36 I. Beretta, F. Rincon, N. Khaled, P. Grassi, V. RANA, D. A. Atienza
Design Exploration of Energy-Performance Trade-Offs for Wireless Sensor Networks
49th Annual Design Automation Conference 2012, DAC 2012, proc. p. 1043-1048, San Francisco, CA, USA, Giugno 2012
Vincitore dell'HiPEAC Best Paper Award

C.37 P. R. Grassi, I. Beretta, V. RANA, D. Sciuto
Tacit Consent: A Technique to Reduce Redundant Transmissions from Spatially Correlated Nodes in Wireless Sensor Networks
15th EUROMICRO Conference on Digital System Design, DSD 2012, proc. p. 874 - 881, Cesme, Izmir, Turchia, Settembre 2012

C.38 P. R. Grassi, I. Beretta, V. RANA, D. Sciuto, D. A. Atienza
Knowledge-Based Design Space Exploration of Wireless Sensor Networks
International Conference on Hardware-Software Codesign and System Synthesis, CODESS+ISSS 12, proc. p. 225-234 , Tampere, Finlandia, Ottobre 2012

C.39 A. Nacci, V. RANA, I. Beretta, F. Bruschi, D. A. Atienza, D. Sciuto
A high-level synthesis flow for the implementation of iterative stencil loop algorithms on FPGA devices
50th Annual Design Automation Conference 2013, DAC 2013,
article n. 52, p. 1-6, Austin, TX, USA, Giugno 2013
Vincitore dell'HiPEAC Best Paper Award

C.40 A. Nacci, V. RANA, M. D. Santambrogio and D. Sciuto
Improving the security and the scalability of the AES algorithm
ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, FPGA 2014, pp. 256, Monterey, CA, USA, Febbraio 2014

C.41 A. Nacci, G. Bettinazzi, C. Pilato, V. RANA, M. D. Santambrogio, D. Sciuto
A SystemC-Based Framework for the Simulation of Appliances Networks in Energy-Aware Smart Spaces
IEEE World Forum on Internet of Things, WF-IoT 2014, pp. 485-490, Seoul, Korea, Marzo 2014

C.42 A. Nacci, V. RANA, D. Sciuto, M. D. Santambrogio
An open-source, efficient and parameterizable hardware implementation of the AES algorithm
12th IEEE International Symposium on Parallel and Distributed Processing with Applications, ISPA 2014, pp. 85-92, Milano, Italia, Agosto 2014

C.43 V. RANA, F. Bruschi, M. Paolieri, D. Sciuto and M. D. Santambrogio
On How to Efficiently Implement Regular Expression Matching on FPGA-based Systems
12th IEEE International Conference on Embedded and Ubiquitous Computing, EUC 2014, pp. 304-309, Milano, Italia, Agosto 2014

C.44 A. Nacci, V. RANA, D. Sciuto
A Perspective Vision on Complex Residential Building Management Systems
12th IEEE International Conference on Embedded and Ubiquitous Computing, EUC 2014, pp. 209-214, Milano, Italia, Agosto 2014

C.45 G. Conte, M. de Marchi, A. Nacci, V. RANA, D. Sciuto
BlueSentinel: a first approach using iBeacon for an energy efficient occupancy

detection system
1st ACM International Conference on Embedded Systems for Energy-Efficient Buildings, BuildSys 2014, pp. 11-19, Memphis, USA, Novembre 2014

C.46 A. Piscitello, A. Nacci, V. RANA, M. D. Santambrogio and D. Sciuto
Sink State Analysis in multi-tenant smart buildings
2nd IEEE International Forum on Research and Technologies for Society and Industry Leveraging a better tomorrow (RTSI)

C.47 A. Piscitello, A. Nacci, V. RANA, D. Sciuto, M. D. Santambrogio
Ruleset minimization in multi-tenant Smart Buildings
14th IEEE/IFIP International Conference on Embedded and Ubiquitous Computing (EUC 2016)

C.48 A. Pagani, F. Bruschi, V. RANA, M. Restelli
Reconstruction of public transport state
19th IEEE Intelligent Transportation Systems Conference (ITSC 2016), pp. 2285 - 2292, Rio de Janeiro, Brazil, November 2016

C.49 P. Cancian, G. W. Di Donato, V. RANA, M. D. Santambrogio
An Embedded Gabor-based Palm Vein Recognition System
2017 IEEE International Conference on Biomedical and Health Informatics of the IEEE Engineering in Medicine and Biology Society (BHI2017), pp. 405-408, Orlando, Florida, USA, February 2017

C.50 A. Pagani, F. Bruschi, V. RANA
Knowledge Discovery from car sharing data for traffic flows estimation
2017 Smart City Symposium Prague (SCSP 2017), pp. 1-6, Prague, Czech Republic, 2017

C.51 A. Pagani, F. Bruschi, V. RANA
Time of Arrival Cumulative Probability in Public Transportation Travel Assistance
20th IEEE Intelligent Transportation Systems Conference (ITSC 2017), *in printing*

C.52 A. Pagani, F. Bruschi, V. RANA, M. Restelli
User Context Estimation for Public Travel Assistance and Intelligent Service Scheduling
20th IEEE Intelligent Transportation Systems Conference (ITSC 2017), *in printing*

5.4 Ph.D. Forum, Workshop, Poster, University Booth and Newsletter

D.1 F. Ferrandi, A. Mele, V. RANA, M. D. Santambrogio, D. Sciuto
A Caronte-oriented approach to a network-based educational infrastructure
6th European Workshop on Microelectronics Education - EWME 06, proc. p. 133 - 136, Stockholm, Sweden, June 2006

D.2 C. Bolchini, C. Brandolese, L. Frigerio, V. RANA, F. Salice, M. D. Santambrogio
RoadRunner and IPGen: a combined solution to speedup the reconfigurable architectures design
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